Altera Technical Solutions Seminar 2000

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Schedule

- Opening
- Introduction
- FLEX® 10KE Devices
- APEX™ 20K & Quartus™ Overview
- Design Integration
- EDA Integration
- Intellectual Property
- Design Iteration
- Design Optimization
- Internet Interface
- Roadmap
- Quartus Demo

Agenda

Introduction

FLEX® 10KE Devices

APEX™ 20K & Quartus™ Overview

Design Integration

EDA Integration

Intellectual Property

Design Iteration

- Incremental Compilation
- SignalTap™ Logic Analysis
- SameFrame™ Pin-Out

Design Optimization

Internet Interface

Roadmap

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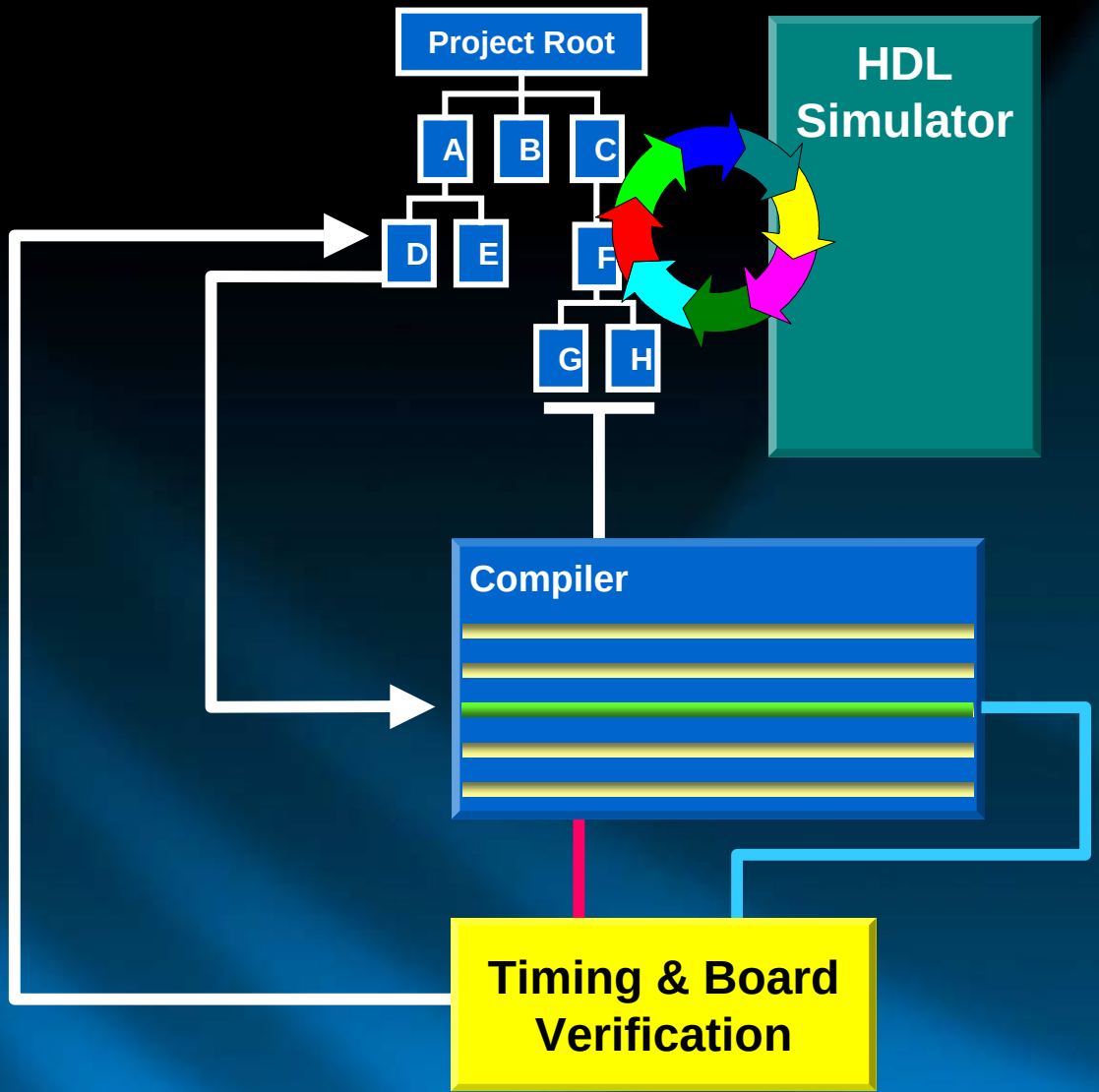
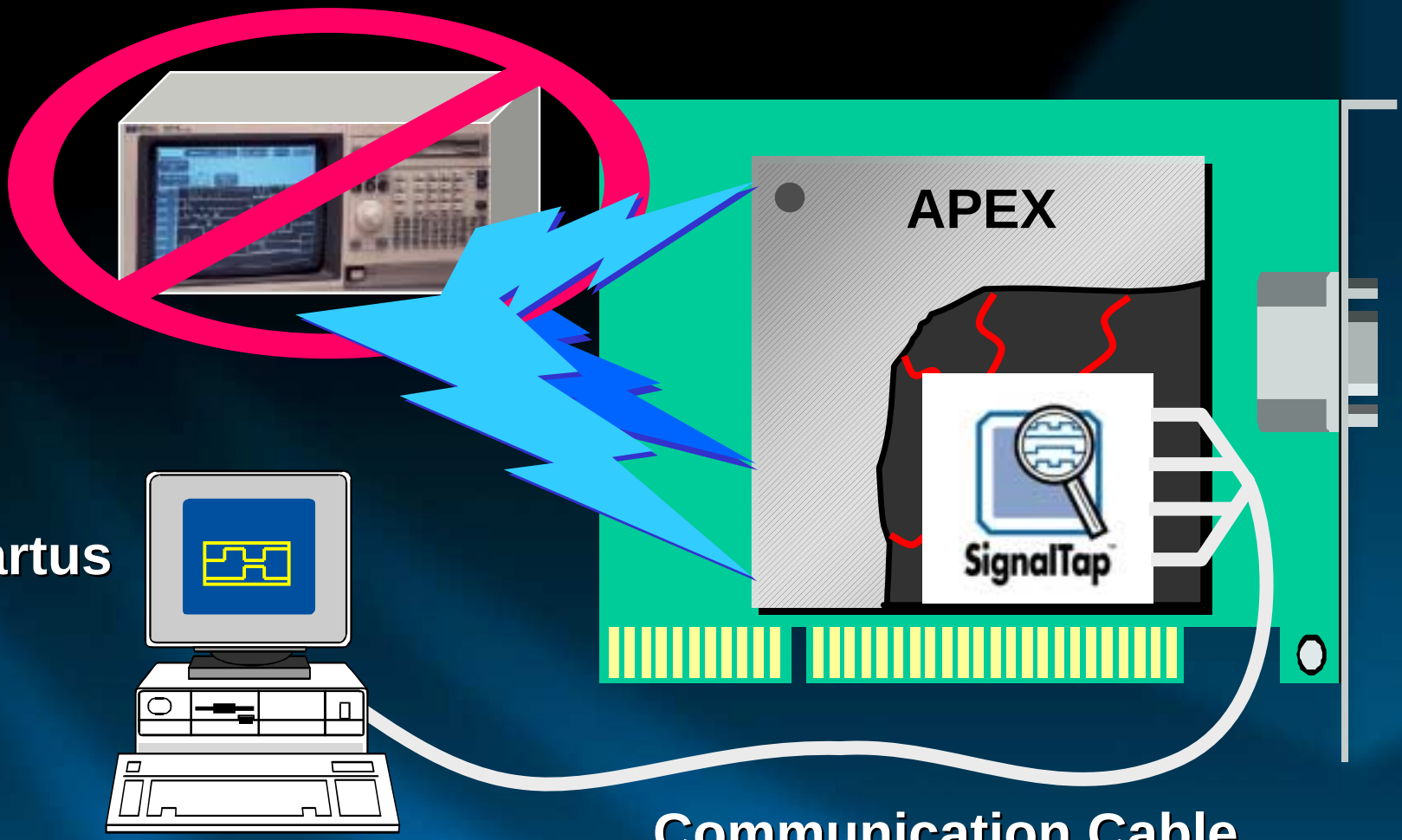
Easy-to-Use Verification Tools

- Integrated HDL Simulator for Verifying Code Before Compilation
- Integrated Gate-Level and Timing-Level Simulation
- Nodes Automatically Located in Source Code
- Easy Integration with Third-Party Verification Tools

Incremental Recompilation

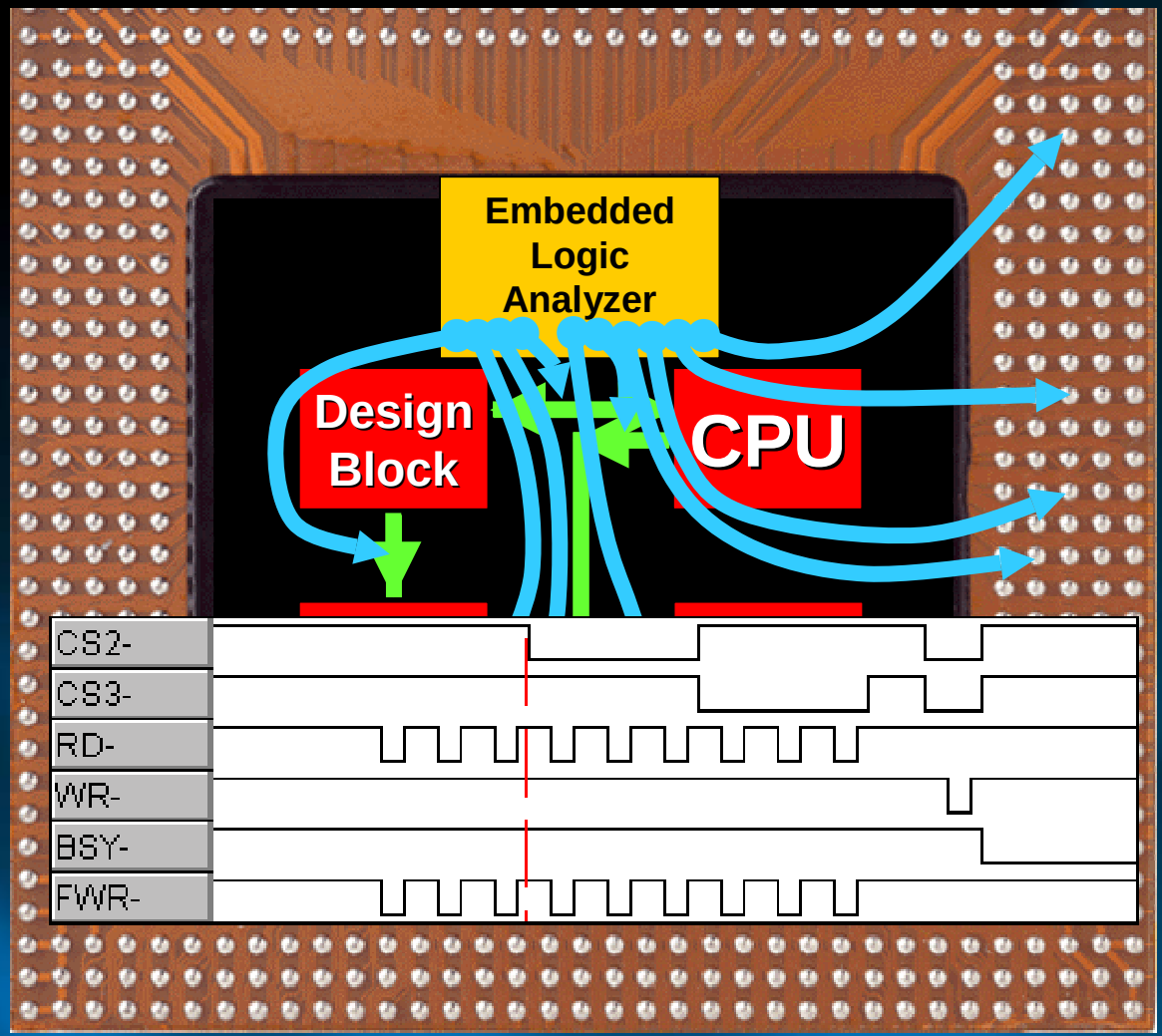


SignalTap™ Logic Analysis



Embedded Logic Analysis

Debugging Internal Logic



Embedded Logic Analyzer

- Parameterized Megafunction
- Integrated with Quartus
  - Signal Selection
  - Trigger Setup
  - Run Control
  - Waveform Display
- Operates at System Speed

Memory Usage

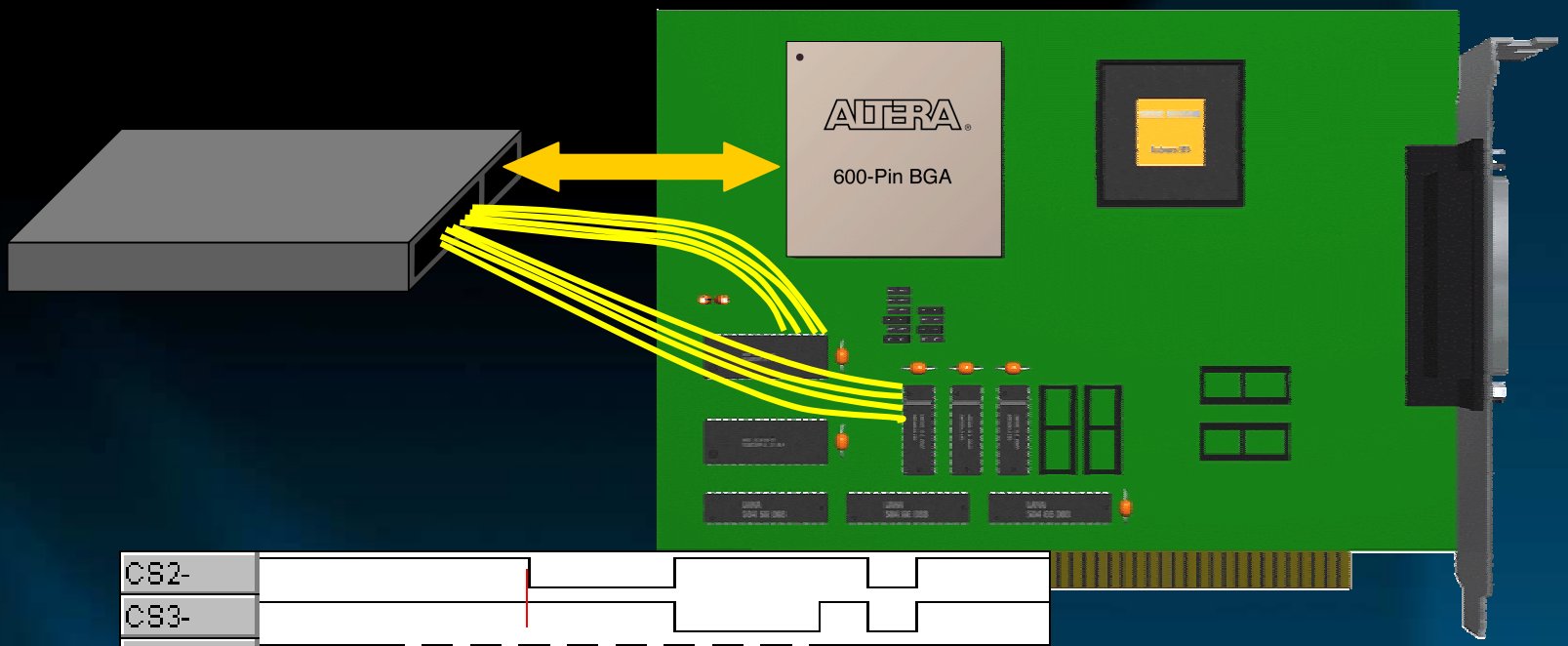
Memory Depth - Samples

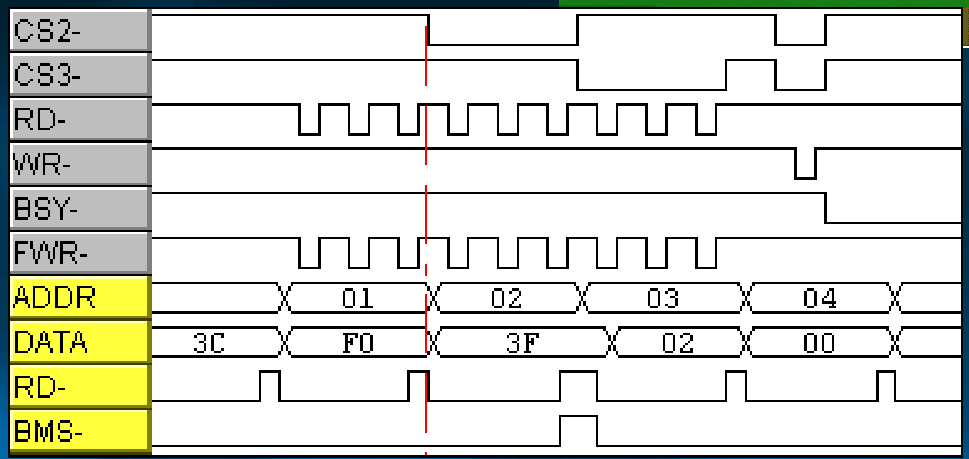
Channels

	128	256	512	1,024	2,048
1	1	1	1	1	1
2	1	1	1	1	2
4	1	1	1	2	4
8	1	1	2	4	8
16	1	2	4	8	16
32	2	4	8	16	32
64	4	8	16	32	64
128	8	16	32	64	128

Device	ESBs
EP20K100	26
EP20K160	40
EP20K200	52
EP20K300	72
EP20K400	104
EP20K600	152
EP20K1000	264

SignalTap Plus





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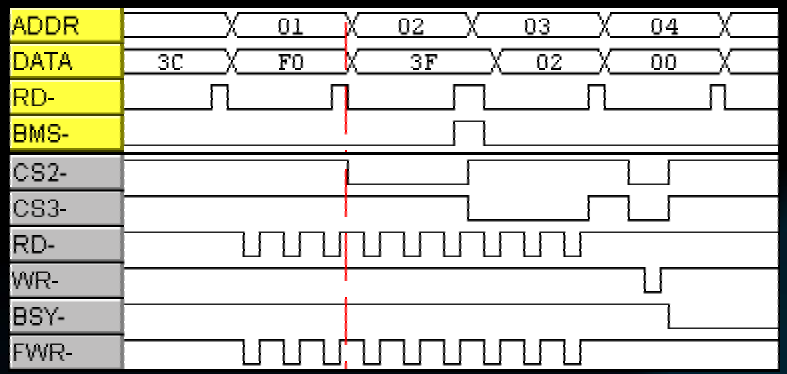
SignalTap Plus System Analyzer



External Board-level Activity

Internal Chip-level Activity

System Centric Debug

MasterBlaster Communications Cable

JTAG

SignalTap

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SignalTap Plus Specifications

- All MasterBlaster capabilities *Plus:*
- 32 channel logic analyzer
  - 1 external clock input
  - 1 trigger output
- 1M samples per channel
- Sample Rate
  - Synchronous - 166 MHz (external clock)
  - Asynchronous - 166 MHz (internal clock)

SignalTap Plus Specifications

- Triggering
  - 4 level sequence
  - Event count (1k occurrences)
  - Pattern duration (1k clocks)
  - Timeout (16M clocks)

Industry Comparison

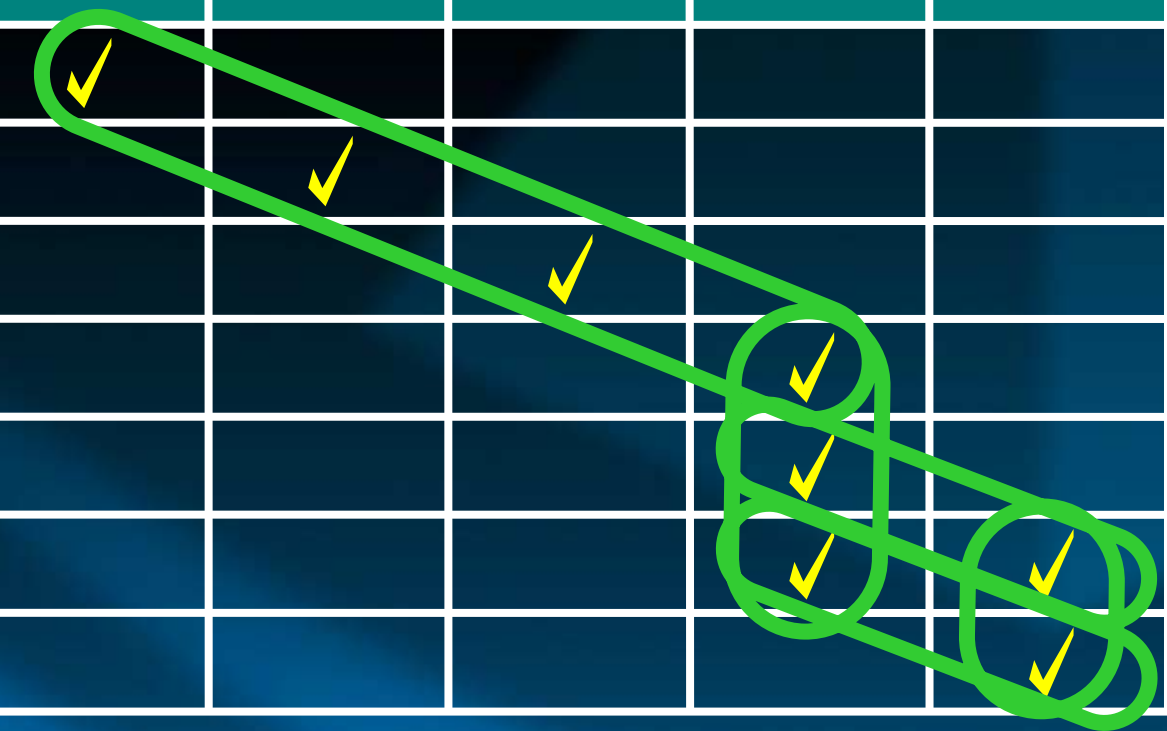
Agilent (HP) LogicWave

APEX 20K SameFrame Support

Device	196-Pin FineLine BGA	324-Pin FineLine BGA	484-Pin FineLine BGA	672-Pin FineLine BGA
EP20K100	✓	✓		
EP20K200			✓	✓
EP20K400				✓

APEX 20KE SameFrame Support

Device	196-Pin FineLine BGA	324-Pin FineLine BGA	400-Pin FineLine BGA	484-Pin FineLine BGA	672-Pin FineLine BGA	900-Pin FineLine BGA
EP20K100E	✓	✓				
EP20K160E			✓			
EP20K200E				✓		
EP20K300E					✓	
EP20K400E					✓	
EP20K600E					✓	✓
EP20K1000E						✓



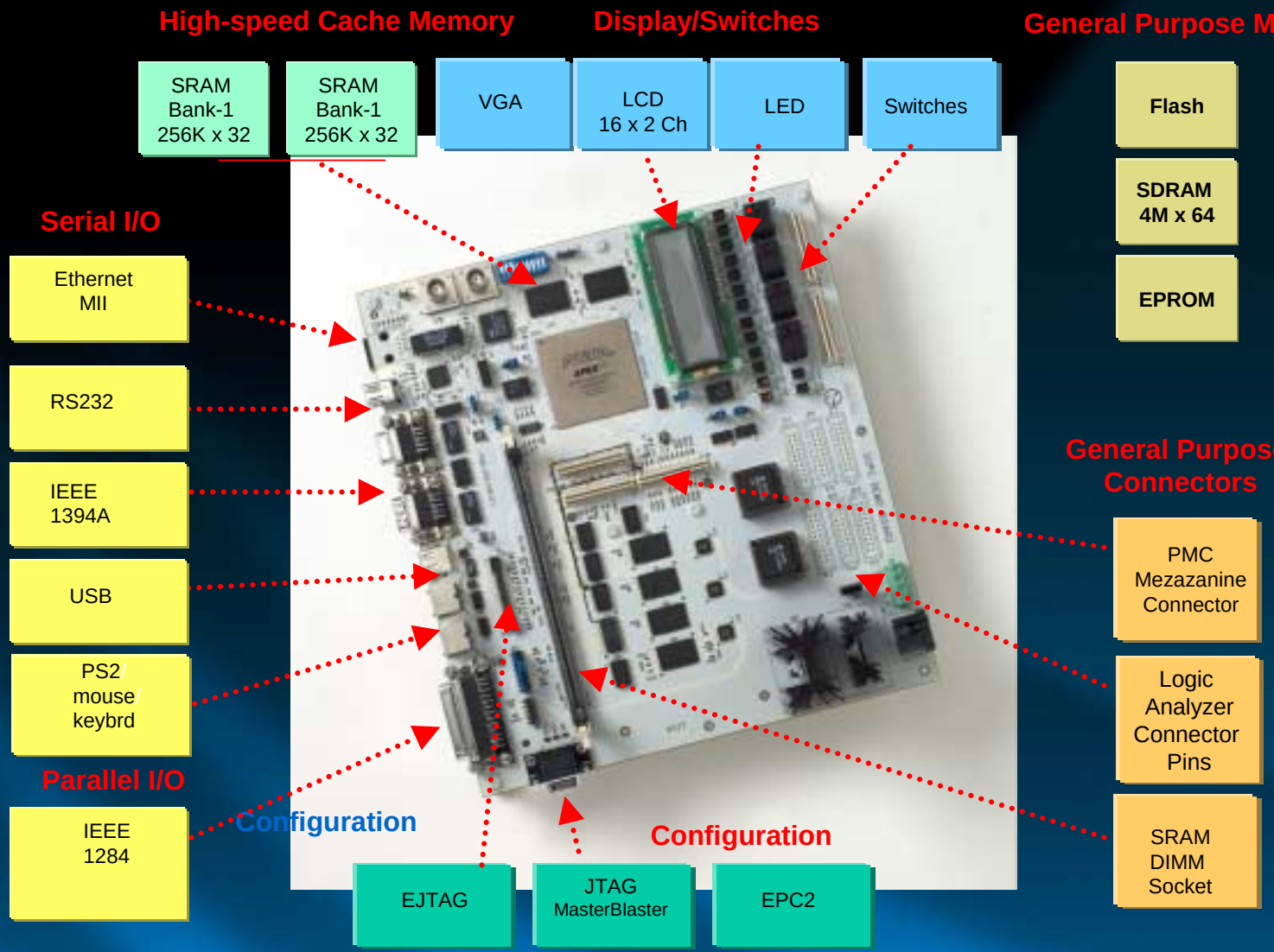
Design Iteration Summary

- Verify Behavior Before Compiling
- Incremental Compilation Speeds Time to Market
  - Changes Made Quickly
  - Compilation Only Performed on Changed Portions of Design
  - More Opportunity to Optimize
- SignalTap/Plus for Real-Time Hardware Debug
- SameFrame Pin-Out for Density, Package Changes

SOPC Development Board Overview

- Complete Hardware Platform for SOPC Design
  - System resources for microprocessor, memory, custom logic, & standard I/Os
- Order code: SOPC-BOARD/A4E
  - APEX 20K400E 652–1
    - Now ships with –1 or –2X
    - Plan to ship with –1X when available
  - Future upgradeable to 20K1500 - 652

Key Feature Overview



Product Overview

- SOPC Development Board product ships with:
  - SOPC Board
  - MasterBlaster™
  - CD ROM
    - User Guide
    - Test cores
    - 99 IP Catalog
    - Link to web info

Product Overview (continued)

- Operates with Altera and AMPP IP
- PCI development using PMC connector only
  - Not in PCI form factor (standalone)
  - APEX PCI board scheduled for 3Q00
- Demonstration programming files (.pof)
  - Posted on IP MegaStore site as available

IP MegaStore