Altera Technical Solutions Seminar 2000

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Schedule

- Opening
- Introduction
- FLEX® 10KE Devices
- APEX™ 20K & Quartus™ Overview
- Design Integration
- EDA Integration
- Intellectual Property
- Design Iteration
- Design Optimization
- Internet Interface
- Roadmap
- Quartus Demo

Agenda

- Introduction
- FLEX® 10KE Devices
- APEX™ 20K & Quartus™ Overview
- Design Integration
- EDA Integration
- Intellectual Property
- Design Iteration
- **Design Optimization**
- Internet Interface
- Roadmap

- Routing Structure
- CoreSyn™ Synthesis
- Floorplanning

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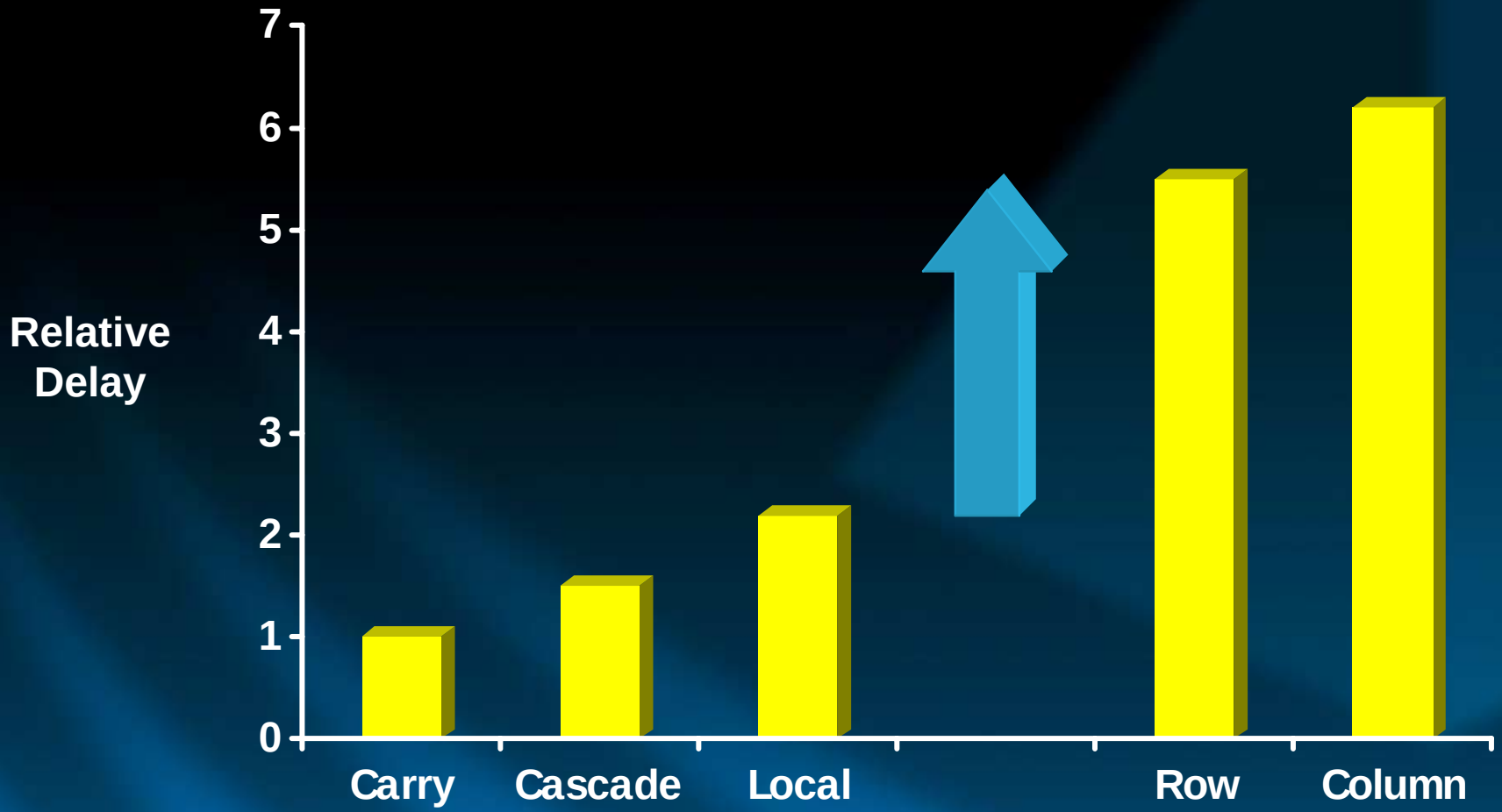
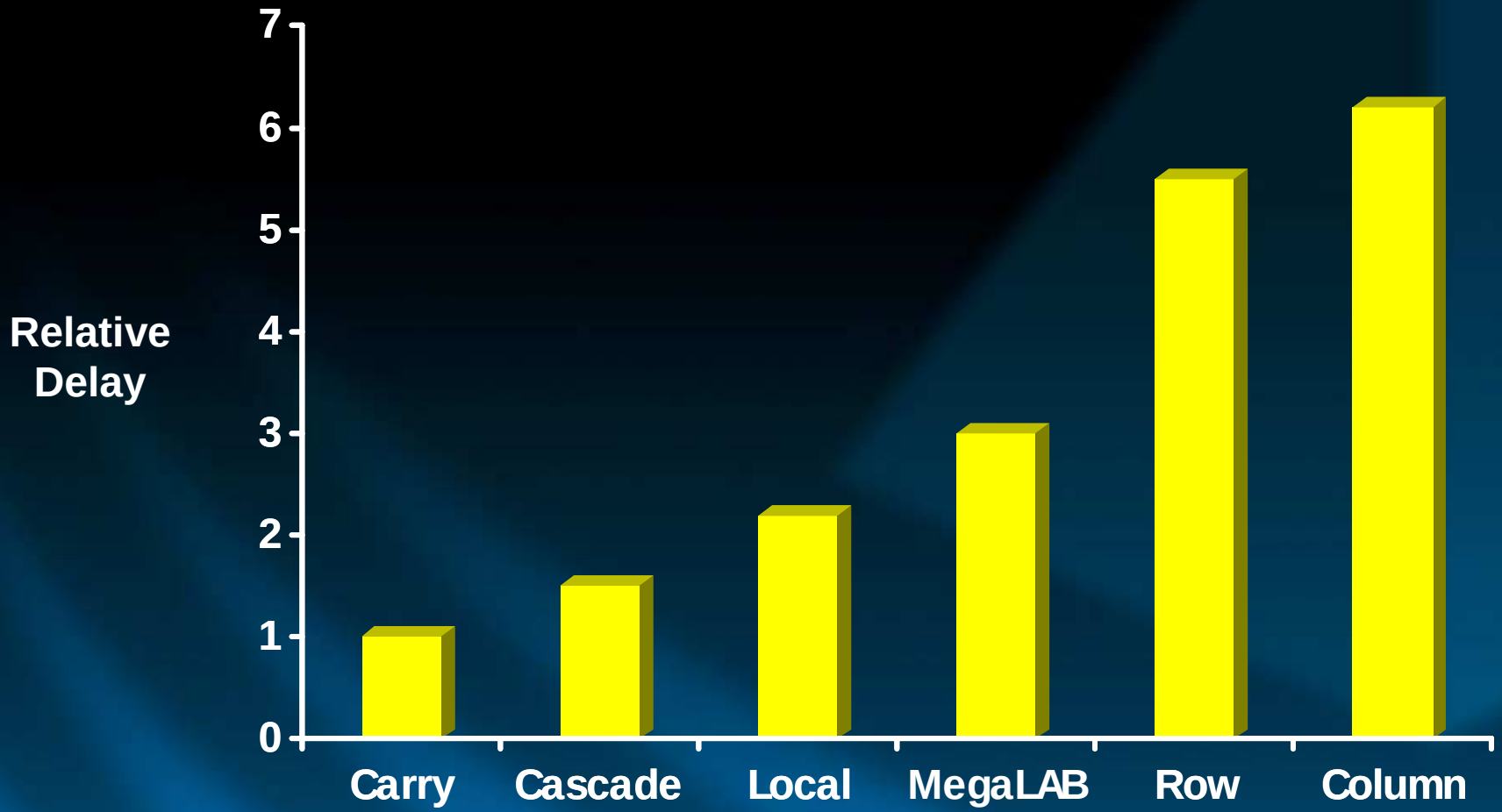
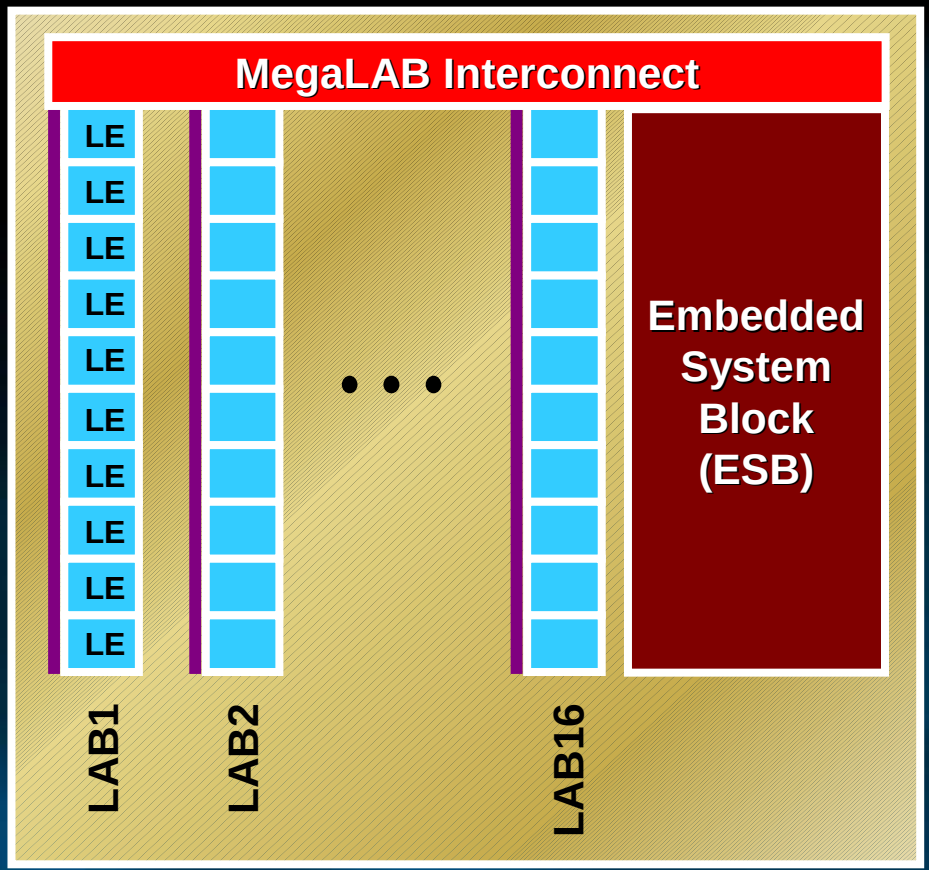
Potential Delay Gap



MegaLAB Level Eliminates Gap



MegaLAB Helps Optimize Speed

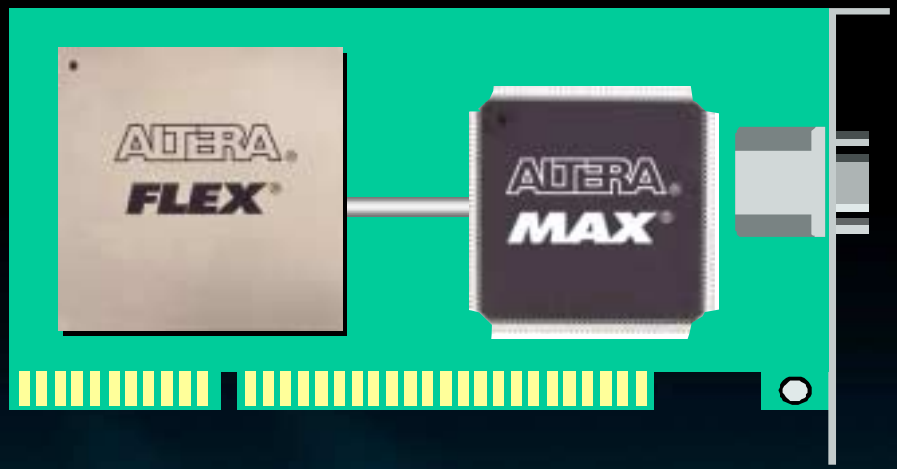


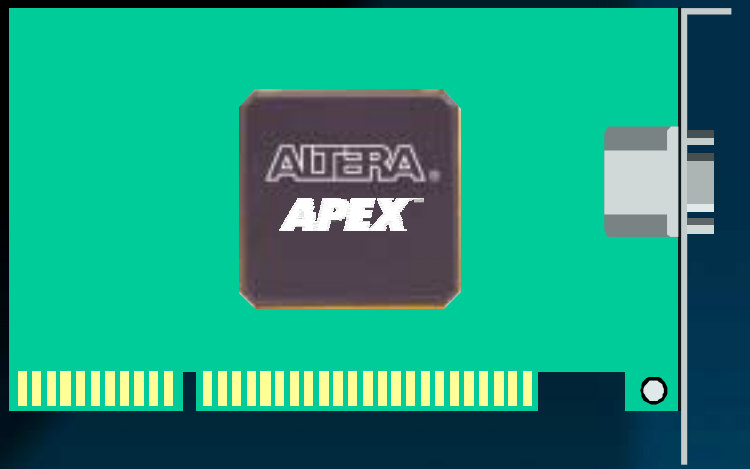
160 LEs of Logic, Plus 2K RAM or 16 Macrocells

MultiCore Performance Benefits

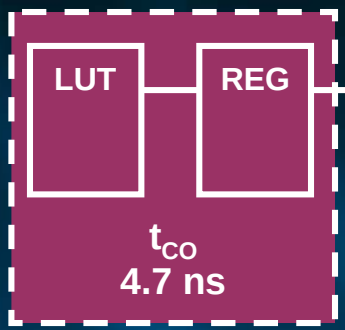
Function	FLEX 10KE	MAX 7000AE	APEX 20K
16-State, 5-Input/ Output State Machine	129 MHz	161 MHz	161 MHz
5 x 5 Registered I/O Multiplier	166 MHz	59 MHz	166 MHz

Embedded Product-Term Performance



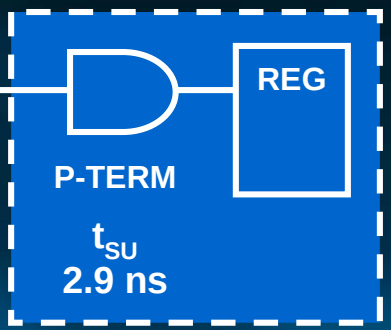


EPF10K100E-1



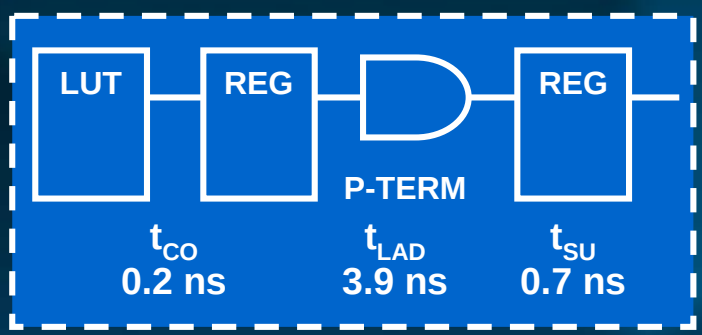
t_D
1.0 ns

EPM7064S-5



8.6 ns

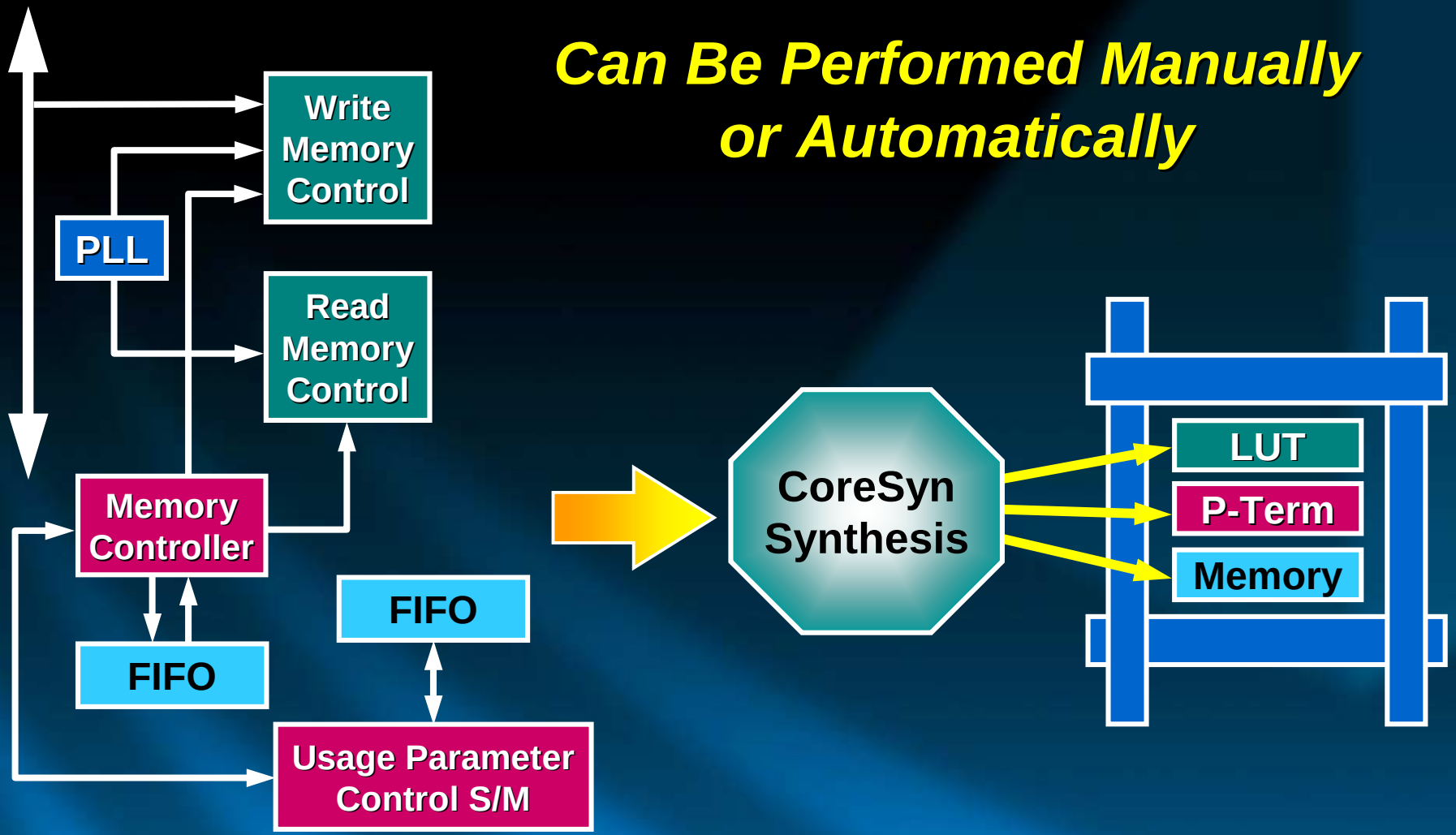
APEX 20K-1 Speed Grade



4.8 ns

CoreSyn™ Synthesis Optimizes Mapping

Can Be Performed Manually or Automatically



Efficient Floorplan Editor

- Flexible Editing Capabilities
  - Multi-Level Undo/Redo
  - Drag-and-Drop Assignments into Other Quartus Windows
  - Grouped Drag-and-Drop
- All Nodes Can Be Automatically Located in Source File

Optimization Summary

- Optimize for Density and/or Performance
- MegaLAB Provides Higher Performance
- CoreSyn Synthesis for Optimal Implementation
- Floorplanner Allows Quick Identification of Paths and Delays