



Altera Technical Solutions Seminar 2000



Schedule

- Opening
- Introduction
- FLEX[®] 10KE Devices
- APEX[™] 20K & Quartus[™] Overview
- Design Integration
- EDA Integration
- Intellectual Property
- Design Iteration
- Design Optimization
- Internet Interface
- Roadmap
- Quartus Demo



Agenda

Introduction

FLEX[®] 10KE Devices

APEX[™] 20K &

Quartus[™] Overview

Design Integration

EDA Integration

Intellectual Property

Design Iteration

● Design Optimization

Internet Interface

Roadmap

u Help

u Service Requests





Industry's First Fully Web-Aware Tool

- ◆ **Quartus Has Internet Connectivity Built-in**
- ◆ **Many Support Issues Handled Automatically**
 - **Device Support Updates**
 - **Patches**
 - **Software Problem Reporting and Tracking**
 - **Enhancement Requests**



Web-Assisted Help

The screenshot shows the Quartus tutor web page in a browser window. The page title is "Quartus - tutor - [http://www.altera.com/demo/area.html]". The browser's address bar shows the URL. The page has a navigation bar with links: Home, Search, Site Map, Devices, Tools, Literature, Atlas, and Contact. Below the navigation bar is a banner for "ALTERA" with sub-links: Solutions, Examples, Articles, Training, and Feedback. The main content area is titled "Problem" and "Solution". The "Problem" section asks: "How can I reduce the logic element (LE) count in my FLEX[®] design?". The "Solution" section states: "There are several steps or settings a designer can use to minimize LE count in [FLEX](#) designs. Some examples are given below:". Below the text is a list of two bullet points: "• Use functions from the library of parameterized modules (LPM) whenever possible for arithmetic and gate functions in the design." and "• Use carry and cascade chains for arithmetic functions. You can use carry and cascade chains for a function either individually or globally, using individual logic options or using **Global Project Logic Synthesis** (Assion menu) respectively". At the bottom of the page, there is a status bar that says "For Help, press F1".

Problem

How can I reduce the logic element (LE) count in my FLEX[®] design?

Solution

There are several steps or settings a designer can use to minimize LE count in [FLEX](#) designs. Some examples are given below:

- Use functions from the library of parameterized modules (LPM) whenever possible for arithmetic and gate functions in the design.
- Use carry and cascade chains for arithmetic functions. You can use carry and cascade chains for a function either individually or globally, using individual logic options or using **Global Project Logic Synthesis** (Assion menu) respectively



Service Requests Web-Enabled

File Edit View Insert Project Compile Tools Window Help

chiptrip

Address http://de183/birchnet/sentry.asp

Altera PRODUCTS SEARCH SUPPORT AUTHORIZATION CODES

ALTERA®

The Quartus Home

Create a Service Request

Information on [how to create an service request](#) is available for your reference.
*Note: Required fields are **highlighted**.*

Choose a Product:

Product:

Specify the Problem:

☐ This problem can be duplicated.
☐ I am working with multiple PC's and this problem occurs on several of them.

Priority

Computer Information:

Operating System:

OS Version:

Computer Make:

Memory (Mb of RAM):

Computer Model:

External EDA Tool:

External EDA Tool Version:

Enter a brief descriptive title for this problem

ASM: LE_USE_CLOCK_ENABLE bits not supported **A fix is available for download**

ASM: Closing databases

ASM: Writing configuration file

ASM: ASM End

Compilation complete

Compile Simulate Timing System

For Help, press F1



Internet Summary

- ◆ Internet Capability Increases Productivity
- ◆ Help Available On-Line
 - Updated in the Factory
 - Context-Sensitive
- ◆ Upgrades Easier to Load
- ◆ File Service Requests Directly from Quartus