



Altera Technical Solutions Seminar 2000

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Schedule

- Opening
- Introduction
- FLEX® 10KE Devices
- APEX™ 20K & Quartus™ Overview
- Design Integration
- EDA Integration
- Intellectual Property
- Design Iteration
- Design Optimization
- Internet Interface
- Roadmap
- Quartus Demo



Agenda

Introduction

FLEX® 10KE Devices

APEX™ 20K &
Quartus™ Overview

Design Integration

EDA Integration

Intellectual Property

Design Iteration

Design Optimization

Internet Interface

Roadmap





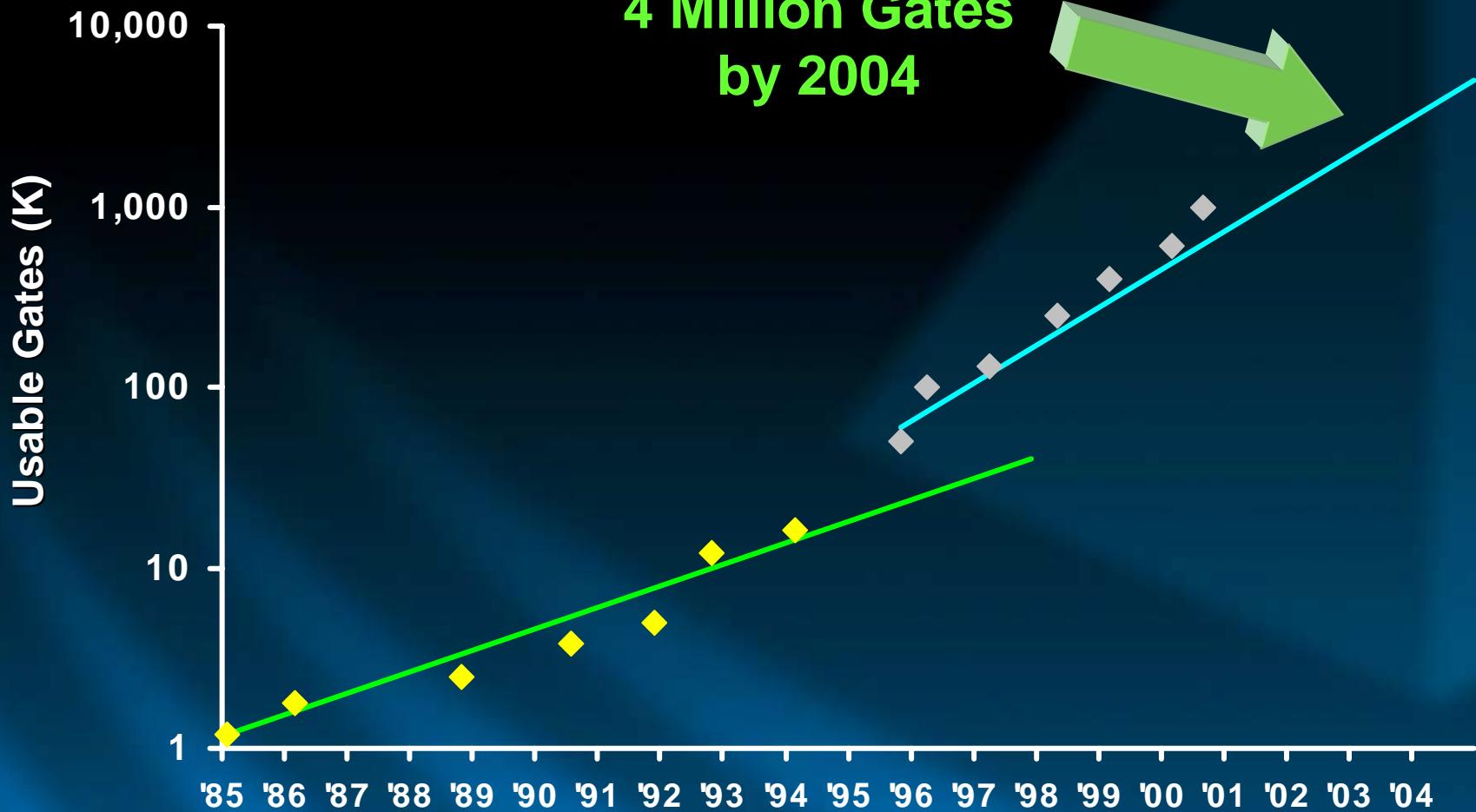
Process Dimensions Trend





Gate Count Roadmap

4 Million Gates
by 2004





BGA Package Roadmap

Size \ Pitch	1.27 mm	1.0 mm	0.8 mm	0.5 mm
27 mm	A green square grid representing a 256-ball BGA package with a 1.27 mm pitch.	A green square grid representing a 676-ball BGA package with a 1.0 mm pitch.	A green square grid representing a 1,024-ball BGA package with a 0.8 mm pitch.	A green square grid representing a 2,500-ball BGA package with a 0.5 mm pitch.
17 mm		A green square grid representing a 256-ball BGA package with a 1.0 mm pitch.		
13 mm			A green square grid representing a 256-ball BGA package with a 0.8 mm pitch.	
9 mm				A green square grid representing a 256-ball BGA package with a 0.5 mm pitch.



Summary

- ◆ **System Integration Places New Demands on PLDs**
 - Millions of Gates
 - Performance Measured in Hundreds of MHz
 - Shorter Time-to-Market
- ◆ **Altera First to Address True System-Level Needs**
 - FLEX 10KE
 - APEX 20K
 - Quartus
 - Megafunctions



FLEX 10KE Devices

FLEX[®] 10KE

- ◆ Driving FLEX 10K Technology
- ◆ 115-MHz Performance
- ◆ 64-Bit, 66-MHz PCI Compliance
- ◆ Dual-Port RAM
- ◆ Performance Tuning Via PLLs
- ◆ Board Savings with FineLine BGAs
- ◆ SameFrame Capability for Design Flexibility
- ◆ 2.5-V Reduces Power Consumption



APEX 20K Family

APEX™

- ◆ A Million Gates
- ◆ 125-MHz
 - 64-Bit, 66-MHz PCI Compliance
- ◆ System-Level Capabilities
 - Optimized Logic Implementations
 - LUT-Based Logic
 - Product-Term-Based Logic
 - DPRAM
 - CAM
 - ClockLock, ClockBoost PLLs
 - Multiple I/O Standards

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Quartus Development System

- ◆ Million-Gate Designs
- ◆ Fits into Third-Party Design Flows
 - NativeLink™ Integration
 - VB and TCL/TK Scripting
- ◆ Design Teams
- ◆ Faster Compiles
- ◆ Incremental Compilation
- ◆ SignalTap™ Logic Analysis
- ◆ Logic in LUTs and Product-Terms
- ◆ Internet Interface



Intellectual Property

- ◆ Altera Provides MegaCore Functions
- ◆ AMPP Partners Offer Wide Array of Functions
- ◆ OpenCore Evaluation Provides Risk-Free Trial
- ◆ MegaWizard Plug-Ins for Easy Implementation



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Now coming!

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Altera Enables a System-on-a Programmable-Chip Solution

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