System on Programmable Chip SoPC for High Performance System Applications
Agenda

- Altera SoPC Roadmap
  - Product Roadmap
  - Packaging Roadmap
  - Tools Roadmap
  - IP Roadmap

- Quartus II, the tool for SoPC class design
  - Quartus II Introduction
  - Quartus II Roadmap
  - Altera Development Tools Strategic Objectives
  - New Feature Details

- High Performance Device solution for SoPC
  - APEXII, Mercury, ACEX, HardCopy(MPLD)

- SoPC Design with Embedded Processors Solution
  - ARM & MIPS Hardcore Embedded Processors
  - Hardcore Processor Design Flow
Altera Product Roadmap
SOPC Strategy

High-Density PLDs

Development Software

Intellectual Property

Design Services
Programmable Logic Capacity

10 Million Gates in 5 years

Beyond APEX

APEX 20K

FLEX 10K

FLEX® 8000

MAX 7000

MAX® 5000

Classic
Process Geometry Migration

- 0.22, 5LM, Al 2.5V
- 0.18, 6LM, Al 1.8V
- 0.15, 8LM, Cu 1.8V/1.5V
- 0.13, 8LM, Cu 1.5V/1.2V
Product-Term Roadmap

MAX 7000: Maximum Performance
MAX 3000: Lowest Cost

0.8µm, 2LM, 5V
0.5µm, 3LM, 5V ISP
0.35µm, 4LM, 3.3V
FineLine BGA
Ultra FineLine BGA
512 Macrocells
0.22µm, 4LM, 2.5V
Advanced I/O

Next Generation product-term architecture
LUT Roadmap

- **2.5M Gates**
  - Beyond APEX II 2001
  - APEX 20KC 2001
  - All layer Cu

- **1.5M Gates**
  - Excalibur 2000
  - Mercury 2001

- **100K Gates**
  - APEX E 1999

- **10K Gates**
  - FLEX 10KE 1998
  - FLEX 10K 1995

- **2.5M Gates**
  - APEX E 1999
  - FLEX 8000 1992

- **1.5M Gates**
  - FLEX 10KE 1998
  - APEX E 1999
  - APEX 10KE 1995

- **100K Gates**
  - FLEX 10K 1995

- **10K Gates**
  - Logic

- **2.5M Gates**
  - Logic
  - Memory
  - PLL

- **1.5M Gates**
  - Logic
  - Memory
  - PLL

- **100K Gates**
  - Logic
  - Memory
  - PLL

- **10K Gates**
  - Logic
  - Memory
  - PLL
Packaging Roadmap
Packaging Roadmap

0.25 μm  →  0.18 μm  →  0.13 μm  →  0.10 μm

Wire-Bonded BGAs  FlipChip BGAs  Multiple Stacked Die  MCMs & Embedded Passives

1.27 mm  1.0 mm  0.8 mm  0.5 mm

PCB

1998  1999  2000  2001  2005

Alterna Advantage

MCM: Multichip Module
LRC: Inductors Resistors Capacitors
BGA Efficiency

- **1.27-mm Ball Pitch**
  - 27 mm: 256 Pins
  - 35 mm: 356 Pins

- **1.0-mm**
  - 17 mm: 256 Pins
  - 27 mm: 672 Pins

- **0.8-mm**
  - 14 mm: 256 Pins
  - 27 mm: 1,024 Pins

- **0.5-mm Ball Pitch**
  - 9 mm: 256 Pins
  - 27 mm: 2,704 Pins
Flip-Chip Technology

- **Wire Bond Die**
  - Bond Pads Located On Periphery
  - Increased Path Length from Bond Pads to Solder Balls
  - Reduced I/O Performance

- **Flip-Chip Die**
  - Solder Bumps Not Restricted to Periphery
  - Path Length from Die to Solder Balls Significantly Reduced
  - Increased I/O Performance
Flip Chip Advantages

- Higher Routing Density
  - 1 dimension pad ring --> 2 dimension pad array

- No More Restricted by Bond Pad Pitch Limit

- Shorter Interconnection
  - Vertical Path
  - Higher Speed
  - Higher Power

- Better Thermal Performance
  - Heatsink/lid/fin can be directly attached to the back of die/package
# BGA Roadmap

<table>
<thead>
<tr>
<th>Size</th>
<th>1.27 mm</th>
<th>1.0 mm</th>
<th>0.8 mm</th>
<th>0.5 mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>27 mm</td>
<td>![Image](256 Balls)</td>
<td>![Image](672 Balls)</td>
<td>![Image](1,024 Balls)</td>
<td>![Image](2,500 Balls)</td>
</tr>
<tr>
<td>17 mm</td>
<td>![Image](256 Balls)</td>
<td>![Image](256 Balls)</td>
<td>![Image](256 Balls)</td>
<td>![Image](256 Balls)</td>
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<tr>
<td>13 mm</td>
<td>![Image](256 Balls)</td>
<td>![Image](256 Balls)</td>
<td>![Image](256 Balls)</td>
<td>![Image](256 Balls)</td>
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<tr>
<td>9 mm</td>
<td>![Image](256 Balls)</td>
<td>![Image](256 Balls)</td>
<td>![Image](256 Balls)</td>
<td>![Image](256 Balls)</td>
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</tbody>
</table>
Tools Roadmap
IP Roadmap
# Intellectual Property Cores

<table>
<thead>
<tr>
<th>Communications</th>
<th>Bus Interface</th>
<th>Digital Signal Processing</th>
<th>Processor, Peripheral</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ethernet MAC</td>
<td>PCI Target</td>
<td>FIR Filter Compiler</td>
<td>Nios™ Processor</td>
</tr>
<tr>
<td>(10/100/Gigabit)</td>
<td>PCI Master-Target</td>
<td>IIR Filter Compiler</td>
<td>Tensilica X-tensa</td>
</tr>
<tr>
<td>SONET Framer</td>
<td>PCI-X</td>
<td>Fast Fourier Transform</td>
<td>Processor</td>
</tr>
<tr>
<td>T3/E3 Framer</td>
<td>CAN Bus</td>
<td>Reed Solomon</td>
<td>PalmChip Bus</td>
</tr>
<tr>
<td>Packet Over SONET</td>
<td>IIC Master &amp; Slave</td>
<td>Encoder/Decoder</td>
<td>SDRAM Controller</td>
</tr>
<tr>
<td>Processor</td>
<td>IEEE 1394</td>
<td>Viterbi Decoder</td>
<td>DDR-SDRAM Controller</td>
</tr>
<tr>
<td>Utopia Master &amp; Slave</td>
<td>PowerPC Bus</td>
<td>Turbo Encoder/Decoder</td>
<td>QDR-SDRAM Controller</td>
</tr>
<tr>
<td>POS-PHY Interface</td>
<td>Arbiter</td>
<td>Interleaver/Deinterleaver</td>
<td>8237 DMA Controller</td>
</tr>
<tr>
<td>HDLC Protocol Core</td>
<td>PowerPC Bus</td>
<td>Digital Modulator</td>
<td>8255 Peripheral</td>
</tr>
<tr>
<td>ADPCMC (u-law, a-law)</td>
<td>Master</td>
<td>NCO</td>
<td>Interface</td>
</tr>
<tr>
<td>ATM Controller</td>
<td>PowerPC Bus Slave</td>
<td>Color Space Converter</td>
<td>8259 Interrupt</td>
</tr>
<tr>
<td>CRC</td>
<td>USB Function Controller</td>
<td>Discrete Cosine Transform</td>
<td>Controller</td>
</tr>
<tr>
<td>IMA Controller</td>
<td>USB Host Controller</td>
<td>Image Processing Library</td>
<td>8254 Timer/Counter</td>
</tr>
<tr>
<td>Telephony Tone Generator</td>
<td></td>
<td></td>
<td>8051, 6502, Z80</td>
</tr>
</tbody>
</table>

And More!
Agenda

- Quartus II Introduction
- Quartus II Roadmap
- Altera Development Tools Strategic Objectives
- New Feature Details
Quartus™ II Development Software

Altera’s Fourth-Generation Development Software
Altera Tools Strategic Objectives

- Increase Design Performance
- Enhance Design Methodology
- Improve Design Verification
- Deliver Results

*The Software You’ve Been Waiting For*
Quartus Software Benefits

Quartus Benefits

- SignalTap™ Logic Analysis
- NativeLink™ Integration
- Intellectual Property
- Tcl Scripting

Quartus II Benefits

- Industry’s Fastest Compile Times
- 30-60% $f_{\text{MAX}}$ Improvement
- SOPC Design Environment
- Superior Designer Productivity
What’s New In Quartus II

- User Interface
- Synthesis & Tech. Mapping
- Place and Route
- Data Structures
- Improved Constraint UI
- PowerFit Technology
- Excalibur APEX 20KC
- Incremental Framework
- PowerGauge™
## Feature Roadmap

<table>
<thead>
<tr>
<th>Q1 2001</th>
<th>Q2 2001</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Quartus II Version 1.0</strong></td>
<td><strong>Quartus II Version 1.1</strong></td>
</tr>
<tr>
<td>- Excalibur SoftMode™</td>
<td>- LogicLock™ v1.0</td>
</tr>
<tr>
<td>- PowerFit Technology</td>
<td>- SOPC Builder v1.1</td>
</tr>
<tr>
<td>- CDR Capability</td>
<td>- Significantly Enhanced NativeLink Integration</td>
</tr>
<tr>
<td>- PowerGauge™ Analysis Software</td>
<td>- Timing Assignment (Wildcard)</td>
</tr>
<tr>
<td>- Project Archive</td>
<td>- Quartus II Baseline</td>
</tr>
</tbody>
</table>

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Feature Roadmap

Quartus II Version 1.2 (Q4 2001)
- LogicLock v1.1
- SOPC Builder v1.2
- 25% Faster Compile Time
- New Assignment Organizer
- More NativeLink Enhancement
- Register Duplication
- SignalTap II Logic Analyzer
## Device Support

<table>
<thead>
<tr>
<th>Quartus II Version 1.0</th>
<th>Quartus II Version 1.1</th>
<th>Quartus II Version 1.2</th>
</tr>
</thead>
<tbody>
<tr>
<td>JAN 2001</td>
<td>JULY 2001</td>
<td>Q4 2001</td>
</tr>
</tbody>
</table>

- APEX 20K
- APEX 20KE
- APEX 20KC
- Excalibur™
- Mercury™
- FLEX® 6000

- APEX 20K
- APEX 20KE
- APEX 20KC
- Excalibur
- Mercury
- FLEX 6000
- APEX II
- ACEX 1K
- FLEX 10KE

- APEX 20K
- APEX 20KE
- APEX 20KC
- Excalibur
- Mercury
- FLEX 6000
- APEX II
- ACEX 1K
- FLEX 10K
- MAX® 7000A
- MAX 7000B
- MAX 3000A
Altera Tools Strategic Objective #1

**Increase Design Performance**
- Top Objective: Elevate Push-Button $f_{\text{MAX}}$ Performance
- I/O Timing Also Critical
- Must Also Enable Performance Optimization (Beyond Push-Button)

**Quartus II Meets Challenge with:**
- New PowerFit Router Technology
  - Delivers 10-20% Faster $f_{\text{MAX}}$
  - Enhances I/O Routing
- APEX 20KC Architecture Provides Another 25-40% Faster $f_{\text{MAX}}$
New Timing-Driven Router

- Complements PowerFit™ (Placement) Technology
Why Do Compile Times Matter?

Compilation Times without PowerFit Technology

Compilation Times with PowerFit Technology

Device Density in Gates

Relative Compilation Time (Hours)
Compile Time Improvement: PowerFit!

- **PowerFit Beta**
- **PowerFit Technology**

Results measured with database of 75 VHDL and Verilog-HDL designs
Quartus II Provides Excellent Stability

Quartus II v1.0
Quartus 2000.09
Quartus 2000.05 SP1

APEX 20KE Devices

Designs up to 95% full
Lower density devices maintain excellent fitting results.
EP20K1500E results are comparable to EP20K1000E
Altera Tools Strategic Objective #2

- **Enhance Design Methodology**
  - Custom Region Assignments
  - Address System Level Design Issues Including Hardware/Software Co-Design
  - Optimize Design Methodology with Incremental Design

- **Quartus II Meets Challenge with:**
  - SoftMode™ Co-Design Feature
  - SOPC Builder (Quartus II v1.1)
  - Incremental Design (Quartus II v1.1)
  - PowerGauge™ Analysis Software
  - Minimum Timing (Quartus II v1.1)
Custom Region Assignments

- Ability to Specify a Rectangular Region for Logic or ESB Placement
- Specify Top Left & Bottom Right Corners of Rectangular Region
  - Boundary is LAB and/or
  - Boundary is ESB
Custom Region Assignments

- Supports Hierarchical Constraints
  - LAB, MegaLAB, ESB Within a Region
- Back-Annotate Assignments Take Precedence Over Custom Region Assignments

Notes
- Custom Region Assignments Do not Appear in Quartus II v1.0
- Cannot Split a LAB
- Cannot Split an ESB
SOPC Builder

**Configured Silicon Features**
(e.g. Memory Mapping)

**Configured IP Cores**

**Interconnect Ports**

**Completed SOPC Architecture**
SOPC Builder Benefits

- “Risk-Free” Architectural Exploration
- Automated IP Integration Flow
- Tremendous Excalibur Demo

Instant Embedded Processor Design!
Quartus II SoftMode™ Co-Design

- Co-Design Capability
- Integrated Software Development Environment
- Generates “Super-POFs” Containing
  - Hardware Bitstreams
  - Software Object Code

![Image of Quartus II Software Settings and User Interface]
PowerGauge™ Analysis Software

- Calculates Power Estimation Based on Simulation File
  - Toggle Rate Derived from User Generated Simulation Vectors
  - Uses Quartus Simulator
  - Accuracy Dependent on Test Vectors
Challenge of Team-Design Methodology

- Multi-Designer Methodology Broken
- IP Methodology Inefficient
- Re-Optimization Highly Unproductive
- Incremental Design Methodology Does Not Work

Introducing LogicLock Incremental Design Capability
LogicLock™ Incremental Design

- Systems On a Programmable Chip Methodology:
  - Modular Design Capability
  - Workgroup Design Capability
  - Improved IP Constraint Capability
  - Incremental Compilation
Design Flows

Current Design Flow

1. Design
2. Integrate
3. Optimize
4. Verify

Modular Design Flow

1. Design-Optimize-Verify Each Module
2. Integrate
3. Optimize-Verify System
LogicLock™ Constraint Types

- **Fixed**
  - Hard Assignment to Specific Location
  - Not Portable Between Devices

- **Floating**
  - LogicLock Chooses the Location
  - Portable Between Devices

- **Relative**
  - Hierarchical Constraint
  - Define Region Constraint Relative to a Higher Level Constraint
  - Portable Between Devices
LogicLock™ Constraint Areas

- Defining Areas
  - User-specified
  - Automatic “Auto-Size”
    - LogicLock Determines Size

- Reserve Areas
  - Can Reserve Area of Device for Future Logic
  - Can Prevent Fitter From Packing Logic In Unused Portion of Region Constraint
Modular Design Capability

- **Optimize Module**
  - Meet Performance
  - Verify Module
- **Lock Down Module**
  - e.g. DSP FIR Filter
- **Add Additional Modules**
  - Performance on DSP FIR Filter Maintained
- **Optimize Additional Modules**
  - Meet Performance
  - Verify Modules
- **Verify System Performance**
## What is Incremental Compilation

<table>
<thead>
<tr>
<th>Incremental Synthesis</th>
<th>Incremental Fitting</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Multiple EDIF/VQM Files</strong></td>
<td><strong>Placement</strong></td>
</tr>
<tr>
<td>User Creates EDIF/VQM for Modules</td>
<td>Hard Lock Nodes to Fitted Lcells in Region</td>
</tr>
<tr>
<td>User Implements Modules with Constraints</td>
<td>Soft Lock Nodes Floating in Region</td>
</tr>
<tr>
<td>User Can Export EDIF/VQM &amp; Constraints</td>
<td>Lock Complete Project</td>
</tr>
<tr>
<td>Recompile Only Modified EDIF/VQMs</td>
<td><strong>Routing</strong></td>
</tr>
<tr>
<td><strong>Synthesize_Separately Option</strong></td>
<td>Routing is Not Lockable</td>
</tr>
<tr>
<td>Synthesizes Only Modified Source Files</td>
<td></td>
</tr>
</tbody>
</table>
3rd Party Synthesis Support

- V1.1 Support
  - Synopsys FPGA-Express
  - Synplicity & Exemplar Require Black-Box Approach
    - Generate Multiple EDIF/VQM
    - Do NOT Use I/O ATOM Mapping at Lower Level Modules

- V1.2 Support
  - Incremental Synthesis Capability in EDA Synthesis Tools
    - Leonardo Spectrum
    - Synplify
LogicLock™ Summary

- Improves Design Performance
  - Synthesis
  - Fitting

- Increases Designer Productivity
  - Supports Iterative Design Process for Multi-clock Domains
  - Enables Workgroup Design
  - Reduced Compilation Time

- Increases Design Reuse
  - Portable Constraints
  - Reduces IP Development Cost
  - Reduces IP Reuse Risks
# EDA Interface Enhancements

<table>
<thead>
<tr>
<th>Quartus II v1.1</th>
<th>Quartus II v1.2</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Toolnet</strong></td>
<td>Timing Analysis</td>
</tr>
<tr>
<td>Cross-probing with Synplicity</td>
<td>Automatic Setup Scripts for PrimeTime</td>
</tr>
<tr>
<td><strong>NativeLink Simulation</strong></td>
<td>Advance Constraint Passing</td>
</tr>
<tr>
<td>Launch Simulator with TB and User Options</td>
<td></td>
</tr>
<tr>
<td>Separate Netlist Writer</td>
<td>Toolnet</td>
</tr>
<tr>
<td></td>
<td>Support for ModelSim with Synplify</td>
</tr>
<tr>
<td></td>
<td><strong>NC-SIM</strong></td>
</tr>
<tr>
<td></td>
<td>Signal Integrity Tools</td>
</tr>
<tr>
<td></td>
<td><strong>Scirocco</strong></td>
</tr>
</tbody>
</table>
Minimum Timing

- Quartus II v1.1 Feature
- Minimum Timing Supported for APEX 20KE Devices
- Feature Enabled via Quartus II User Interface
- Quartus II Provides Verification Output Netlist
  - Generates Maximum & Minimum Timing .vo,.vho & .sdo Netlists
- Native Quartus II Timing Analyzer Provides Support
Tcl Improves Designer Productivity

- Scripts Available on Internet
  - Optimize I/O Timing
  - Lock Down Blocks & Paths
  - Optimize Performance

- Harness Power of Quartus
  - App Note 118: Scripting with Tcl in Quartus
Altera Tools Strategic Objective #3

- **Improve Design Verification**
  - Enhance Board Level Verification
  - Deliver Superior EDA Tool Integration
  - Provides PLD Industry’s Best Timing Analysis Solution

- **Quartus II Meets Challenge with:**
  - Enhanced SignalTap (Quartus II v1.1) Provides Vehicle for Re-thinking Verification Bottleneck
  - NativeLink Delivers Full Cross-Probing Functionality & Provides Enhanced Synthesis Results (Quartus II v1.1)
  - Quartus II Provides Top Native Timing Analysis Tool & Delivers Stamp Interface to PrimeTime
Enhancing SignalTap

- Quartus II v1.0 Provides Fix to Enable SignalTap to Work with PowerFit Technology
- Quartus II v1.1 LogicLock™ Capability Enhances SignalTap
  - Accelerates Viewing Additional Nodes
  - Accelerates Entire Debug Process
- Quartus II v1.2 Adds Ability to Select Nodes in HDL, Dramatically Enhancing Usability of SignalTap
Improved Nativelink Flows - H1 2001

Enhancements for Synthesis Tools:
- Improved Error Location and Cross-probing Between Quartus and Synthesis Tools
- Better Timing Estimates and Timing Closure to Optimize Performance

Enhancements for Simulation Tools:
- Independent Netlist Writer (Ability to Generate a Simulation Netlist without Re-compiling)
- Pass User Specified Testbench and Command Line Options to the Simulation Tool
- Improved Error Location and Cross-probing Between Quartus and Simulation Tools
Quartus II on UNIX Platforms

Improving Performance and Usability
Quartus II on UNIX

- Simplified Installation
- New Database Manager
- New Operating Systems Supported
  - Solaris 2.8
  - HP-UX 11.0
- Advanced Device Support
  - Mercury™ The Programmable ASSP
  - Excalibur™ Embedded Processor Solutions
- Reduced Patch Requirements
## Operating System Availability

<table>
<thead>
<tr>
<th>PC</th>
<th>Quartus II v1.0 Release Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>Windows NT</td>
<td>February 2, 2001</td>
</tr>
<tr>
<td>Windows 2000</td>
<td>February 2, 2001</td>
</tr>
<tr>
<td>Windows 98</td>
<td>February 2, 2001</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>UNIX</th>
<th>Quartus II v1.0 Release Date</th>
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</thead>
<tbody>
<tr>
<td>Solaris 2.8</td>
<td>March 2001</td>
</tr>
<tr>
<td>Solaris 2.7</td>
<td>March 2001</td>
</tr>
<tr>
<td>Solaris 2.6</td>
<td>March 2001</td>
</tr>
<tr>
<td>HPUX 11.0</td>
<td>April 2001</td>
</tr>
<tr>
<td>HPUX 10.2</td>
<td>April 2001</td>
</tr>
</tbody>
</table>
Agenda

- APEX™ II Device Family Overview
- Device Features
  - LVDS Details
  - Embedded System Blocks (ESBs)
  - External Memory Integration
  - Additional Features
- Applications
- Summary
APEX II: The Next Generation

**I/O Capabilities**
- 1-Gbps LVDS, LVPECL, PCML & HyperTransport*
- Up to 124 High Speed Differential I/O Channels
- RapidIO, Utopia IV, CSIX, POS-PHY Level 4
- HSTL, SSTL-2/3
- Programmable Output Drive

**Logic Resources**
- Up to 89,280 Logic Elements
- Up to 1,524-Kbits RAM
- Over 1,000 I/O Pins

**Memory**
- Dual-Port+ For Bi-directional Read & Write Ports
- 4-Kbit Memory Blocks
- External Memory Interface Support for ZBT, DDR & QDR

* Formerly Known as Lightning Data Transport (LDT)
APEX 20KE/C Overview
APEX 20KE & APEX 20KC Overview

- Up to 1.5-Million Usable Gates
- 1.8-V, 0.18µm Process Technology
- All-Layer Copper Interconnect (APEX 20KC)
- True-LVDS™ at 840 Mbps
- 200-MHz System Performance
- Up to 442 Kbits of Embedded RAM
- Advanced I/O Standard Support Including SSTL-2/3, GTL+, CTT, HSTL, LVPECL
- Up to 4 High-Performance PLLs
- Content Addressable Memory (CAM)
# APEX 20KE & APEX 20KC Overview

<table>
<thead>
<tr>
<th>Device</th>
<th>Maximum Gates</th>
<th>Typical Gates</th>
<th>Logic Elements</th>
<th>RAM Blocks</th>
<th>RAM Bits</th>
<th>Max. User I/O 20KE / 20KC</th>
</tr>
</thead>
<tbody>
<tr>
<td>EP20K30E</td>
<td>112,704</td>
<td>30,000</td>
<td>1,200</td>
<td>12</td>
<td>24,576</td>
<td>128</td>
</tr>
<tr>
<td>EP20K60E</td>
<td>161,792</td>
<td>60,000</td>
<td>2,560</td>
<td>16</td>
<td>32,768</td>
<td>196</td>
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<tr>
<td>EP20K100E/C</td>
<td>262,912</td>
<td>100,000</td>
<td>4,160</td>
<td>26</td>
<td>53,248</td>
<td>246 / 252</td>
</tr>
<tr>
<td>EP20K160E</td>
<td>404,480</td>
<td>160,000</td>
<td>6,400</td>
<td>40</td>
<td>81,920</td>
<td>316</td>
</tr>
<tr>
<td>EP20K200E/C</td>
<td>525,824</td>
<td>200,000</td>
<td>8,320</td>
<td>52</td>
<td>106,496</td>
<td>376 / 382</td>
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<tr>
<td>EP20K300E</td>
<td>728,064</td>
<td>300,000</td>
<td>11,520</td>
<td>72</td>
<td>147,456</td>
<td>408</td>
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<tr>
<td>EP20K400E/C</td>
<td>1,051,648</td>
<td>400,000</td>
<td>16,640</td>
<td>104</td>
<td>212,992</td>
<td>488 / 502</td>
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<tr>
<td>EP20K600E/C</td>
<td>1,537,024</td>
<td>600,000</td>
<td>24,320</td>
<td>152</td>
<td>311,296</td>
<td>588 / 624</td>
</tr>
<tr>
<td>EP20K1000E/C</td>
<td>1,771,520</td>
<td>1,000,000</td>
<td>38,400</td>
<td>160</td>
<td>327,680</td>
<td>708 / 708</td>
</tr>
<tr>
<td>EP20K1500E/C</td>
<td>2,391,184</td>
<td>1,500,000</td>
<td>51,840</td>
<td>228</td>
<td>422,368</td>
<td>808 / 808</td>
</tr>
</tbody>
</table>
Mercury™

The Programmable ASSP

Built For Bandwidth
Agenda

- The Programmable Application-Specific Standard Product (ASSP)
- Mercury™ Devices Product Overview
- Mercury I/O Features
- Mercury Core Features
SONET/SDH Semiconductors

Increasing Demand for Higher Bandwidth Systems

Source: Dataquest Forecast

© 2001 Altera Corporation
Historic System Partitioning

- Backplane
- ASSP
- DSP
- SRAM
- Flash
- DRAM
- PLD
- Processor
- Parallel Backplane Communication
- Chip-to-Chip Communication
- Line-Side Communication
- Optical/Analog

© 2001 Altera Corporation
Today’s System Components
Serial Transmission Advantages

- Higher Performance
- Lower Power
- Increased Noise Immunity
- Reduced Board Space

LVTTL
20 Pins at 42 MHz

LVDS
2 Pins at 840 Gbps
The Clock Skew Challenge

As Frequencies Increase, Margin for Clock Skew Disappears
# CDR: The I/O Performance Solution

## Single-Ended I/O Standards

<table>
<thead>
<tr>
<th>Speed</th>
<th>100 MHz</th>
<th>250 MHz</th>
</tr>
</thead>
</table>

### Single-Ended Standards Hit Noise Limitations at ~250 MHz

## Differential I/O Standards (LVDS)

<table>
<thead>
<tr>
<th>Speed</th>
<th>100 Mbps</th>
<th>250 Mbps</th>
<th>500 Mbps</th>
<th>750 Mbps</th>
<th>1 Gbps</th>
</tr>
</thead>
</table>

### Clock Skew Overwhelms Differential I/O Standards at ~1 Gbps

## Clock Data Recovery (CDR)

<table>
<thead>
<tr>
<th>Speed</th>
<th>100 Mbps</th>
<th>250 Mbps</th>
<th>500 Mbps</th>
<th>750 Mbps</th>
<th>1 Gbps</th>
</tr>
</thead>
</table>

### CDR Eliminates Barriers at 1.25 Gbps & Beyond
Clock Data Recovery (CDR)

- Differential Signaling Allows High Clock Speeds
- CDR Takes It To The Next Level
  - Higher Speeds
  - Fewer Signals
  - Better Noise Immunity
  - Better Reliability
  - Lower Power

Differential Signaling

Embed Clock in Data

Transmit Single Stream

Recover Clock from Data

Clock Recovery Unit

Data + Clock

1 Differential Pair

Data

Clock

© 2001 Altera Corporation
Additional CDR Benefits

Without CDR

Carefully Matched Trace Lengths

Difficult to Manage Multiple Clocks

Difficult to Align Clocks with Data

With CDR

Clock Encoded with Data
The Mercury Solution

= 1.25 Gbit CDR + PLD

125 Mbps
1.25 Gbps Data

125 Mbps
1.25 Gbps Data

The Programmable ASSP
CDR Solutions

**Standard ASSPs**
- Limited Channels (Typically 1-4)
- Consumes Board Space Rapidly
- Inflexible – Single Protocol, Fixed Functionality
- Power Hungry, Costly Process Technologies

**Mercury™**
- Up to 18 Channels
- Integrated with Programmable Logic
- Fully Flexible – Address Multiple Common Standards & Proprietary Designs
- Production CMOS Process Technology
# Common Mercury Applications

<table>
<thead>
<tr>
<th>Application</th>
<th>Bandwidth (Mbps)</th>
<th>Channels</th>
<th>Mercury</th>
</tr>
</thead>
<tbody>
<tr>
<td>SONET Standards</td>
<td>9,953</td>
<td>8</td>
<td>✓</td>
</tr>
<tr>
<td>POS-PHY L4</td>
<td>9,953</td>
<td>8</td>
<td>✓</td>
</tr>
<tr>
<td>RapidIO</td>
<td>8,000</td>
<td>16</td>
<td>✓</td>
</tr>
<tr>
<td>Gigabit Ethernet</td>
<td>1,250</td>
<td>Any</td>
<td>✓</td>
</tr>
<tr>
<td>IEEE 1394</td>
<td>1,200</td>
<td>Any</td>
<td>✓</td>
</tr>
<tr>
<td>Fibre Channel</td>
<td>1,062</td>
<td>Any</td>
<td>✓</td>
</tr>
<tr>
<td>High-Definition Television</td>
<td>742.5</td>
<td>Any</td>
<td>✓</td>
</tr>
<tr>
<td>Proprietary Backplanes</td>
<td>Any</td>
<td>Any</td>
<td>✓</td>
</tr>
</tbody>
</table>

**Mercury Supports**

**Wide Variety of Common Standards**
High-Speed Serial Backplanes

- High-End Systems Exceed PCI Capabilities
- CDR Enables Multi-Crystal Operation
- CDR Enables High-Speed Backplanes

**Standardized**
Common Protocols & Implementations

**Proprietary**
Differentiation & Value Proposition for System Architects

- Backplane
- Mercury Device
- Serial Backplane Connection
- Multiple Line Cards with Independent Clocks
Altera Content Expansion
CDR Performance Roadmap

CDR Enables Gigabit Performance

Shipping Today!

1.25 Gbps
2.5 Gbps
3.125 Gbps
10 Gbps
Mercury Product Overview
Mercury Product Family

- CDR I/O Performance at 1.25 Gbps
- High-Performance I/O Capabilities
- Performance-Optimized Architecture

Mercury™

The Programmable ASSP

Built For Bandwidth
Family Overview

- Architecture Developed from the Ground Up for High-Bandwidth Functions
  - High-Speed CDR
  - New Core Architecture
  - Additional I/O Features

<table>
<thead>
<tr>
<th>Device</th>
<th>CDR Channels</th>
<th>Typical Gates</th>
<th>Logic Elements</th>
<th>ESBs</th>
<th>RAM Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>EP1M120</td>
<td>8</td>
<td>120,000</td>
<td>4,800</td>
<td>12</td>
<td>48K</td>
</tr>
<tr>
<td>EP1M350</td>
<td>18</td>
<td>350,000</td>
<td>14,400</td>
<td>28</td>
<td>112K</td>
</tr>
</tbody>
</table>
Mercury Features

- 1.8-V, 0.15-μm, 8-Layer-Metal, All-Layer-Copper SRAM Process
- Up to 350K Gates
  - Up to 18 Channels of CDR
  - Up to 14,400 Logic Elements (LEs)
  - Up to 115,000 Bits of RAM
- Ground-Breaking I/O Performance
  - CDR at up to 1.25 Gbps with LVDS, LVPECL & PCML
  - PCI, PCI-X, HSTL, SSTL, GTL+, AGP, LVTTL, LVCMOS & Others
  - ZBT, QDR, DDR RAM Support
  - Flip-Chip Packaging Technology
  - Advanced Phase-Locked Loops (PLLs)
Mercury Features

- Speed-Optimized Core Performance
  - Priority Interconnect
  - Distributed Multiplier Feature
  - Quad-Port RAM
Core Performance Improvements

Core Performance*

* Estimated Design Performance

FLEX
## Core Performance Improvements

### Significant Performance Benefits in Common Functions

<table>
<thead>
<tr>
<th>Function</th>
<th>APEX</th>
<th>Mercury</th>
</tr>
</thead>
<tbody>
<tr>
<td>16-Bit Loadable Counter</td>
<td>264 MHz</td>
<td>333 MHz&lt;sup&gt;(1)&lt;/sup&gt;</td>
</tr>
<tr>
<td>32-Bit Loadable Counter</td>
<td>239 MHz</td>
<td>335 MHz&lt;sup&gt;(2)&lt;/sup&gt;</td>
</tr>
<tr>
<td>32-to-1 Multiplexer</td>
<td>-</td>
<td>1.67 ns</td>
</tr>
<tr>
<td>32 x 64 Asynchronous FIFO</td>
<td>156 MHz</td>
<td>311 MHz</td>
</tr>
<tr>
<td>16 x 16 Non-Pipelined Multiplier</td>
<td>73 MHz</td>
<td>130 MHz</td>
</tr>
</tbody>
</table>

<sup>(1)</sup> Limited to Device Clock $f_{\text{MAX}}$ of 333 MHz, Critical Delay = 1.9 ns (526 MHz)

<sup>(2)</sup> Limited to Device Clock $f_{\text{MAX}}$ of 333 MHz, Critical Delay = 2.13 ns (469 MHz)
All-Layer Copper Technology

1.8-V, 0.15-µm, 8 Layer-Metal All-Layer Copper Process

Advantages

- High Performance
- Excellent Conductor of Electricity
- Scalability Allows Faster Technology Shrinks
- Simpler Process Technology than Aluminum
- Better Electromigration & Reliability
Mercury I/O Features
Advanced I/O Capabilities

- Up to 18 Channels of 1.25-Gbps CDR
- Flexible-LVDS™ Circuitry on All Pins
- 200-MHz ZBT SRAM & 332-Mbps DDR SDRAM Interfaces
- HSTL, PCI-X & Other I/O Standards
- High-Performance Flip-Chip Packaging
- Up to 12 PLL-Generated Clocks
- Enhanced Clock Structures
CDR Capability

- Dedicated High-Speed CDR Circuitry
- 1.25 Gbps per Channel, 45 Gbps Total CDR Bandwidth
- Multiple Differential Standards
  - LVDS
  - LVPECL
  - PCML
- Independent PLL & Serialization Factors
  - Serializers/Deserializers (SERDES) Support Factors from 3 to 20
  - CDR-Dedicated PLLs Support Multiplication Factors from 1 to 20
- Push-Button Software Implementation
The Programmable ASSP

**CDR Transceiver ASSP**

- Addresses Only One Protocol
- Additional Logic

**Mercury™**

- Addresses Any Protocol
- Additional Logic

**Dedicated Circuitry**

**Programmable Logic**
CDR Receiver Data Flow

Encoded Serial Data Stream

Serial to Parallel

Sync

J-Bit Data

Re-Timed J-Bit Data

J-Bit Symbol

M-Bit Data

J-Bit Data

Re-Timed J-Bit Data

M-Bit Data

Serial to Parallel

Sync

Align

Decode

Internal Symbol Clock

Recovered Clock to Core

Reference Clock

Dedicated Circuitry

Programmable Logic

PLL

Clock Recovery

÷J

Recovered Clock

÷J

Recovered Clock

Recovered Clock to Core
CDR Transmitter Data Flow

M-Bit Data → Encode

J-Bit Symbol → Encode

Encode → Sync

Parallel to Serial

÷J

PLL

Transmit Clock

Reference Clock

Encoded Serial Data Stream

Programmable Logic

Dedicated Circuitry

Internal Symbol Clock
Rate-Adaptive CDR

- Mercury CDR Offers Unmatched Flexibility
  - Fully Rate-Adaptive
  - Supports Any Frequency from 125 Mbps to 1.25 Gbps
  - Two Different Serial Data Rates Supported Simultaneously
    - Support Provided by Two Independent CDR-Dedicated PLLs

LVDS @ 1.25 Gbps
LVPECL @ 622 Mbps

LVPECL @ 622 Mbps
LVDS @ 1.25 Gbps
Mercury Flexible-LVDS™

- Additional Support for Differential Standards
- LVDS Available on Every Pin
  - Over 100 Channels on EP1M350
- LVDS Buffers Built into I/O Cell
  - No External Components Needed
- Data Rates of up to 432 Mbps

Note: Available on EP1M350 Only
### Advanced I/O Standard Support

<table>
<thead>
<tr>
<th>I/O Standard</th>
<th>Applications</th>
<th>Approximate Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVDS + CDR</td>
<td>Line Side &amp; Backplane</td>
<td>1.25 Gbps</td>
</tr>
<tr>
<td>LVPECL + CDR</td>
<td>Clock Distribution</td>
<td>1.25 Gbps</td>
</tr>
<tr>
<td>PCML + CDR</td>
<td>High Speed</td>
<td>1.25 Gbps</td>
</tr>
<tr>
<td>LVDS</td>
<td>Backplane &amp; Point to Point</td>
<td>840 Mbps</td>
</tr>
<tr>
<td>1.5-V HSTL I, II</td>
<td>Cache RAMs/ Fast SRAMs</td>
<td>125 - 250 MHz</td>
</tr>
<tr>
<td>SSTL-3 I, II</td>
<td>SDRAMs</td>
<td>80 - 166 MHz</td>
</tr>
<tr>
<td>SSTL-2 I, II</td>
<td>DDR SDRAMs</td>
<td>160 - 332 Mbps</td>
</tr>
<tr>
<td>GTL+</td>
<td>Backplane Driver</td>
<td>200 MHz</td>
</tr>
<tr>
<td>3.3-V 1x/2x AGP</td>
<td>Graphic Processors</td>
<td>66 MHz</td>
</tr>
<tr>
<td>CTT</td>
<td>JEDEC Standard</td>
<td>N/A</td>
</tr>
<tr>
<td>3.3-V PCI</td>
<td>PC, Embedded</td>
<td>64 bit / 66 MHz</td>
</tr>
<tr>
<td>3.3-V PCI-X</td>
<td>PC, Embedded</td>
<td>64 bit / 133 MHz</td>
</tr>
<tr>
<td>3.3-,2.5,1.8-V LVTTL</td>
<td>General purpose</td>
<td>250 MHz</td>
</tr>
</tbody>
</table>
External Memory Support

- Complete High Performance Memory Solution
  - Large Memory Requirements
    - Built-in ZBT, QDR & DDR Interfaces
  - Small to Medium Memory Requirements
    - Enhanced On-Board Embedded System Blocks
## External Memory Support

- Dedicated Support for Emerging High-Speed Memory Standards
  - Performance Targeted for Future Devices

<table>
<thead>
<tr>
<th>Memory Type</th>
<th>$V_{CCIO}$</th>
<th>Specifications (I/O Standards)</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZBT SRAMs</td>
<td>3.3 V / 2.5 V</td>
<td>LVTTL</td>
<td>200 MHz</td>
</tr>
<tr>
<td>QDR SRAMs</td>
<td>1.5 V</td>
<td>HSTL</td>
<td>664 Mbps</td>
</tr>
<tr>
<td>DDR SRAMs</td>
<td>1.5 V</td>
<td>HSTL</td>
<td>332 Mbps</td>
</tr>
<tr>
<td>DDR SDRAMs</td>
<td>2.5 V</td>
<td>SSTL-2 (I/II)</td>
<td>332 Mbps</td>
</tr>
<tr>
<td>SDR SDRAMs</td>
<td>3.3 V</td>
<td>SSTL-3 (II)</td>
<td>166 MHz</td>
</tr>
<tr>
<td>Synchronous SRAMs</td>
<td>3.3 V / 2.5 V</td>
<td>LVTTL</td>
<td>166 MHz</td>
</tr>
</tbody>
</table>
Double Data Rate I/O

- Double Data Rate I/O Circuitry
  - Clock Data on Both Rising & Falling Edge
  - Dedicated Circuitry Provides Robust DDR Support
  - I/O Support on All Pins up to 332 Mbps

Diagram:
- Clock
- Data0
- Data1
- Data2
- Data3
- Data4
- Data5
DDR Implementation

- Output Enable Register Becomes Second Data Register
- Dedicated Latch Ensures Proper Data Recovery
**Phase-Locked Loop (PLL)**

- **Simplified Clock Management Capabilities**
  - Reduces Design Complexity
    - Skew Minimization
    - Frequency Synthesis
    - Phase Adjustment
    - Flexible Hold-Time Control

- **Enabling Features**
  - ClockLock™ Circuitry
  - ClockBoost™ Circuitry
  - ClockShift™ Circuitry
  - Board-Level Clock Management
Mercury PLL

Locked Clock Outputs Can Drive Fast & Clock Lines

\[ F_{OUT} = F_{IN} \left( \frac{m}{n} \right) k \]

\[ F_{OUT} = F_{IN} \left( \frac{m}{n} \right) p \]

\[ F_{OUT} = F_{IN} \left( \frac{m}{n} \right) q \]

\[ F_{OUT} = F_{IN} \left( \frac{m}{n} \right) v \]

(External)

Input Clock

\( \div n \)

\( \div m \)

Phased Comparator

Voltage-Controlled Oscillator

\( \div k \)

\( \div p \)

\( \div q \)

\( \div v \)

Locked Clock Outputs

Time Delay/Shift

Phase Shift Circuitry

Feedback Clock
Flip-Chip Technology

- Wire Bond Die
  - Bond Pads Located on Periphery
  - Increased Path Length from Bond Pads to Solder Balls
  - Reduced I/O Performance

- Flip-Chip Die
  - Solder Bumps Not Restricted to Periphery
  - Path Length from Die to Solder Balls Significantly Reduced
  - Increased I/O Performance
I/O Flexibility: I/O Banks

- Multiple I/O Banks
  - Enables Simultaneous Communication with Several Devices
    - Multiple I/O Standards
    - Multiple I/O Voltages

Diagram:
- LVDS with CDR
- Cache RAM
- HSTL
- PCI-X
- DDR SDRAM
- SSTL-2
- Backplane
- PC System
Additional I/O Features

- Three I/O Element Registers
  - Fast Setup & Clock-to-out Times
- Bus Hold
- Programmable Pull-Up Resistor
- Programmable Input Delay
  - Fine-Grained Setup & Hold Time Window Adjustment
- Open Drain Output Option
- Programmable Drive Strength
  - 2 mA, 4 mA, 8 mA, 12 mA, 16 mA, 24 mA, PCI, PCI-X
- Programmable Slew Rate
Mercury Core Features
Feature-Rich Architecture

Larger, Quad-Port Memory Blocks

High-Performance Architecture
- Prioritized Routing Structure
- Wider Buses
- Improved Local Routing
- Enhanced Logic Elements (LEs)
- Enhanced Carry Chains

Distributed Multiplier Capability
New Mercury Interconnect Types

New High-Speed Interconnect Channels
Improve Performance
Distributed Multiplier Feature

- Logic Structure Built for Dedicated Multiplier Mode
  - Device Capacity for up to 90 8x8 Multipliers
  - > 130 MHz Performance in 16x16 Mode
  - Dedicated Multiplier Mode in LE
  - Dedicated Routing Paths

- Automatically Implemented by Quartus™ II Software

Key Function for Wireless Communications Applications
Multiplier Implementation

Quartus™ II Floorplan
Mercury Logic Element

Optimized for Speed
Embedded System Block (ESB)

Enhanced ESB Structure

- Quad-Port RAM
  - Bidirectional Dual-Port RAM
  - Dual-Port RAM
  - Single-Port RAM
  - CAM
  - ROM
Quad-Port RAM

Quad-Port RAM Capability Enhances Performance
- Addresses Complex Memory Requirements
- Superior to Slower or More Complex Emulation Methods
- Addresses Bidirectional Dual Port Mode
Quad-Port RAM Applications

- Extensive Support for Multi-Port Applications

Quad-Port
- Microprocessor Cores
- Microprocessor Register Files
- Fibre Channel Interface
- Data Concentrators
- Routers
- Multiple Independent FIFOs
- Modulators
- Caching Applications
- Processor to Processor Communication
- Frame Buffer Processing

Dual-Port
- ROMs
- Arbitrated FIFOs
- Bi-Synchronous FIFOs
- Microprocessor Core
- Register Files
- Fibre Channel Interface
- Quad-Port RAM Applications

Extensive Support for Multi-Port Applications
ESB Partitioning

- Partition Single ESB into Two Blocks
  - Increase Total Number of Memory Blocks per Device
Content-Addressable Memory (CAM)

- CAM Accelerates Fast Search Applications
  - Functions as a Parallel Comparator
  - Order of Magnitude Faster than RAM (Serial)
- Looks up Data in Memory & Outputs Addresses
- Each ESB Supports 2-Kbit CAM (64 Words x 32 Bits)

![Diagram of CAM](image)

Common in High-Speed Communication Applications
The Programmable ASSP

- Communications ASSP Integration
  - Functionality of ASSPs with Flexibility of PLDs
  - System-on-a-Programmable-Chip (SOPC) Solution for High-Performance Transceivers

- Built for Bandwidth
  - Support for I/O Standards, Memory Interfaces
  - Flip-Chip Technology
  - Flexible, High Performance PLL
  - Quad-Port Embedded System Blocks (ESBs)
  - Accelerated Core Performance
ACEX™ Device Families

Low-Cost, High-Performance Solutions for the Communications Marketplace
Agenda

- ACEX Overview
- ACEX Applications
- ACEX 1K Family
- Next-Generation ACEX Families
- The ACEX Advantage
ACEX Overview

Communications Marketplace

- Low-Cost, High-Performance Applications Need Programmable Solution for High-Volume Use
- ACEX is a Broad-Based Programmable Solution
  - Architectures
  - Voltages
  - Feature Sets
AECX Applications

Communications Marketplace

- High-Volume Use in Price-Sensitive Applications
  - Cable & xDSL Modems
  - Low-Cost Switches & Routers
  - Remote Access Concentrators
- High Compounded Annual Growth Rate (CAGR) Opportunities in Marketplace
ACEX Applications

- xDSL Modems
- Cable Modems
- Access Routers
- Low Cost Ethernet LAN Switches
- Remote Access Concentrators
ADSL Modem: Block Diagram

- **ATM PHY (25 Mbps)**
- **Protocol (ASSP or Controller)**
  - *ATM SAR*
  - *Management (Can Be Separate)*
- **Transceiver (1 or 2 ASSPs)**
  - *CODEC*
  - *Data Pump - DMT - CAP*
- **Line Driver (Bipolar & Hybrid)**

- **Ethernet Transceiver 10-Base-T**
- **Flash 1 Mbyte**
- **DRAM/SRAM 1 Mbyte**

- **Video**
- **Cat 3/5 Twisted Pair**
- **Telephone Twisted Pair**
ADSL Modem: Block Diagram

- **ATM PHY (25 Mbps)**
- **Ethernet Transceiver 10-Base-T**
- **Flash 1 Mbyte**
- **DRAM/SRAM 1 Mbyte**
- **Line Driver (Bipolar & Hybrid)**
- **ACEX**

- **Video**
- **Cat 3/5 Twisted Pair**
Remote Access Controller: Block Diagram

- CPU 32/64 Bit
  * Protocol
  * Addressing
  * Management

- WAN Line
  * Port 1
    * 56K Modem
    * ISDN Modem
    * ADSL
    * SDSL
    * T/E Carrier Transceivers/Data Pumps

- Flash
  * Code Store
    2-4 Mbytes

- DRAM/SRAM
  * Buffer
    4-8 Mbytes

- ACEX
The ACEX Solution

- Low-Cost, High-Performance Architecture
  - High-Volume Applications in Communications Marketplace
- Multiple Families at Multiple Voltages
- Pricing
  - Establish Price Leadership in Low-Cost Marketplace

Low-Price Leader
ASIC Replacement

- ACEX Family is The ASIC Replacement Solution
  - Cost-Competitive with ASICs
  - All the Benefits of a Complete Programmable Solution
    - Fast Time-to-Market
    - Design Flexibility
    - Reprogrammability
    - Advanced Development Tools
    - Drop-in Intellectual Property
  - No ASIC Risks. No ASIC NREs. No ASIC Restrictions.
ASSP Replacement

■ Advanced Feature Sets Eliminate Specialized ASSPs
  – Advanced PLLs
  – High-Speed FIFOs & Dual-Port RAM
  – Full 64-Bit, 66 MHz PCI Compliance
  – Advanced I/O Standards
  – MultiVolt I/O Capability

■ Integrate ASSP Functionality into a Low-Cost PLD
  – Save Device Cost
  – Save Board Cost
  – Save Board Development Cost
Altera Redundancy Feature

- Altera-Patented Technology for Application to PLDs
- Significant Yield Improvement
The ACEX Roadmap

- Multiple Families Across Multiple Voltages
  - 2.5-V ACEX 1K Family Available March 2000
  - Future ACEX Families 2001 and Beyond
    - Improved Processes, Higher Densities, Lower Voltages, Enhanced Features
ACEX 1K Family

- **Altera Process Advantage**
  - Hybrid Process
    - 0.22 \( \mu \)m Transistors
    - 0.18 \( \mu \)m Metal Interconnect
    - Maintains 2.5-V Core Operating Voltage
    - Provides Key Cost Improvements
  - Yield Improvements
    - Smaller Die Size Improves Yield
  - Patented Redundancy Feature

- **Availability**
  - Samples Available Now
  - Software Support in MAX+PLUS\(^\text{R}\) II ver. 9.6
ACEX 1K Features

- 64-Bit, 66-MHz PCI Compliant
- PLL Support
  - ClockLock™ Synchronization Circuitry
  - ClockBoost™ Multiplication Circuitry
  - Simultaneous ClockLock & Clock x2 Outputs
- Embedded Dual-Port Memory Blocks
  - 4 Kbit RAM Blocks
- MultiVolt™ I/O Interface
  - 5-V Tolerant I/O
ACEX 1K Features

Dual-Port RAMs & FIFOs
Wr Data  Rd Data
16 16

MultiVolt I/O Interface
5-V Tolerant I/Os

PLL Capability
CLK  CLKx2
ClockLock  ClockBoost

64-Bit, 66-MHz PCI

ACEX 1K
<table>
<thead>
<tr>
<th>Feature</th>
<th>EP1K10</th>
<th>EP1K30</th>
<th>EP1K50</th>
<th>EP1K100</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical Gates</td>
<td>10,000</td>
<td>30,000</td>
<td>50,000</td>
<td>100,000</td>
</tr>
<tr>
<td>Logic Elements</td>
<td>576</td>
<td>1,728</td>
<td>2,880</td>
<td>4,992</td>
</tr>
<tr>
<td>RAM Bits</td>
<td>12,288</td>
<td>24,576</td>
<td>40,960</td>
<td>49,152</td>
</tr>
<tr>
<td>User I/O Pins (Max)</td>
<td>130</td>
<td>171</td>
<td>249</td>
<td>333</td>
</tr>
<tr>
<td>Package Options</td>
<td>100-Pin TQFP</td>
<td>144-Pin TQFP</td>
<td>144-Pin TQFP</td>
<td>208-Pin PQFP</td>
</tr>
<tr>
<td></td>
<td>144-Pin PQFP</td>
<td>208-Pin PQFP</td>
<td>208-Pin PQFP</td>
<td>256-Pin BGA&lt;sup&gt;1&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td>208-Pin PQFP</td>
<td>256-Pin BGA&lt;sup&gt;1&lt;/sup&gt;</td>
<td>256-Pin BGA&lt;sup&gt;1&lt;/sup&gt;</td>
<td>484-Pin BGA&lt;sup&gt;1&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td>256-Pin BGA&lt;sup&gt;1&lt;/sup&gt;</td>
<td>484-Pin BGA&lt;sup&gt;1&lt;/sup&gt;</td>
<td>484-Pin BGA&lt;sup&gt;1&lt;/sup&gt;</td>
<td></td>
</tr>
</tbody>
</table>

Available in MAX+PLUS II v9.6

(1) 256 & 484-Pin Packages Are 1.0-mm FineLine BGA™

Available in MAX+PLUS II v9.6
## The ACEX I/O Advantage

- Communications Applications Require High I/O Counts
  - Allows High Performance Communication
  - Provides Wide Bandwidth Capabilities

<table>
<thead>
<tr>
<th>Device</th>
<th>EP1K10</th>
<th>EP1K30</th>
<th>EP1K50</th>
<th>EP1K100</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max I/O</td>
<td>130</td>
<td>171</td>
<td>249</td>
<td>333</td>
</tr>
</tbody>
</table>
High-Performance Dual-Port RAM

- Independent Read/Write Ports
  - Synchronous/Asynchronous Access
  - 6.5-ns Access Time

- Wide Range of Configuration Options
  - 4 KBits/EAB for Flexibility
  - Width up to x16 for Maximum System Bandwidth

- Fast & Effective FIFO Implementation

```
EAB

<table>
<thead>
<tr>
<th>WRADDRESS</th>
<th>RDADDRESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>DATA</td>
<td>Q</td>
</tr>
<tr>
<td>WREN</td>
<td>RDEN</td>
</tr>
<tr>
<td>WRCLOCK</td>
<td>RDCLOCK</td>
</tr>
</tbody>
</table>
```
ClockLock: Improve I/O Performance

- ClockLock Feature Increases I/O Performance

<table>
<thead>
<tr>
<th></th>
<th>$t_{co}$</th>
<th>$t_{su}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Without PLL</td>
<td>5.2</td>
<td>2.0</td>
</tr>
<tr>
<td>With PLL</td>
<td>4.2</td>
<td>1.5</td>
</tr>
</tbody>
</table>

Note: ACEX 1K Data from MAX+PLUS II ver. 9.6

Improved Timing
ClockBoost - Time-Domain Multiplexing

- Multiplied Clock Used to Share Resources

**Diagram Description:**
- Dataa1[15..0]
- Datab1[15..0]
- Dataa2[15..0]
- Datab2[15..0]
- Control Signal
- clk

**Required LEs Table:**

<table>
<thead>
<tr>
<th>Design</th>
<th>Without ClockBoost</th>
<th>With ClockBoost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Two 16 x 16 Multipliers</td>
<td>1,160</td>
<td>680</td>
</tr>
<tr>
<td>Four 16 x 16 Multipliers</td>
<td>2,320</td>
<td>873</td>
</tr>
</tbody>
</table>
Next-Generation ACEX Families

- Smaller and Improved Processes
- More Enhanced Features
- Lower Costs per Feature
- Lower Voltages
- Higher Densities
- Embedded Dual Port Memory Blocks
- Advanced PLLs
- Advanced I/O Standard Support
- PCI Compliance
- Advanced Development Tools Support
PCI Market Status

- PCI is the Industry’s Bus Standard for Open Systems
  - Emerging I/O Standard for Embedded Applications

- 64-Bit, 66-MHz PCI Required for High-Performance Systems
  - High-Performance Communications Applications
  - Gigabit Ethernet, Fiber Channel
  - High-End Systems Require 64-Bit Addressing

- PCI-X is the Next-Generation Solution
  - Frequencies of up to 133 MHz

Fully 66-MHz/64-Bit PCI & PCI-X Compliant!
Altera PCI Solutions

Megafunctions
- 32- & 64-Bit
- 33- & 66- MHz
- PCI-X

The Altera PCI Solution

Devices
- ACEX 1K
- ACEX 2K

Verification
- Test Vectors
- Hardware Testing

Tools
- MAX+PLUS II
- Quartus
- OpenCore Evaluation
- MegaWizard™ Plug-Ins
- Test Benches
ACEX Summary

- The Premier Programmable Low-Cost Communications Solution
  - Low-Cost for High-Volume Use
  - High-Performance Capabilities for Communications Applications
  - Feature-Rich Architectures
  - Software & Intellectual Property Leadership

ACEX: The Low-Cost, High-Performance Communications Solution
ACEX Applications

- Cable Modems
- xDSL Modems
- Remote Access Systems
  - Remote Access Concentrators
- Private & Branch Access Routers
- Low-Cost Switches
- Low-Cost Line Cards
- Laser Printers
- PC Peripherals
Market Success Factors

- Low Cost & Time-to-Market Critical for Success

Factors Influencing Market Success

- Reducing Cost
- Increasing Functionality
- Reducing Time to Market
- Increasing System Speed
- Increasing Quality/Reliability
- Increasing Ease of Use
- Reducing Form Factor
- Reducing Power Dissipation

Source: Dataquest
ACEX Time-to-Market Advantage

- Quick to Prototyping
  - In-System Design Verification
  - Dramatically Reduced Simulation & Verification Time
  - No Test Vectors Required
  - No Prototype Lead-Times

- Quick to Production
  - No Lengthy Sign-off Cycle
  - No Production Lead Times
ACEX Pricing vs. ASIC Pricing

- Competitive with ASIC Unit Cost
- Benefits of Programmable Logic
  - Faster to Market
  - Low Risk
  - No NRE
  - No Re-Spin Cost
  - Short Lead Times
  - Low Inventory Cost

ACEX Provides Low-Cost Flexibility
Total Cost vs. ASICs

- Total Cost = Device Unit Cost + Development Cost + Hidden Costs
- ACEX Minimizes Hidden Costs
  - No NRE Cost
  - No Lost Opportunity Cost
  - No Re-Spin Cost
  - Low Inventory Cost

<table>
<thead>
<tr>
<th>Total Cost ($)</th>
<th>ACEX</th>
<th>ASICs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device Unit Cost</td>
<td>Development Cost</td>
<td>Development Cost</td>
</tr>
<tr>
<td>Lost Opportunity</td>
<td>NREs</td>
<td>Hidden Costs</td>
</tr>
</tbody>
</table>
### ACEX Summary

#### ACEX Low-Cost Flexibility

<table>
<thead>
<tr>
<th>Item</th>
<th>ASIC</th>
<th>ACEX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device Cost</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Total Cost</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td>Design Flow</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>No NRE</td>
<td>-</td>
<td>✓</td>
</tr>
<tr>
<td>Time-to-Market</td>
<td>-</td>
<td>✓</td>
</tr>
<tr>
<td>In-System Design Verification</td>
<td>-</td>
<td>✓</td>
</tr>
<tr>
<td>No Test Vectors</td>
<td>-</td>
<td>✓</td>
</tr>
<tr>
<td>No Re-Spin Cost</td>
<td>-</td>
<td>✓</td>
</tr>
<tr>
<td>Low Inventory Risk</td>
<td>-</td>
<td>✓</td>
</tr>
</tbody>
</table>
ACEX & APEX Applications

- xDSL Modem
- Remote Access Concentrators
- Ethernet LAN Switch
- Layer 3 Switch
- Central Office Switch
- WAN Router
ACEX 1K Price Advantage

<table>
<thead>
<tr>
<th>ACEX</th>
<th>Cents / Logic Element</th>
</tr>
</thead>
<tbody>
<tr>
<td>EP1K10</td>
<td>0.61</td>
</tr>
<tr>
<td>EP1K30</td>
<td>0.41</td>
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<tr>
<td>EP1K50</td>
<td>0.31</td>
</tr>
<tr>
<td>EP1K100</td>
<td>0.24</td>
</tr>
</tbody>
</table>

Note: End-2000 Pricing in High Volume Quantities

ACEX is The Industry’s Lowest Price Per Function
HardCopy - (New MPLD Program)
Introducing Altera MPLDs

- High-Volume, Low-Cost Roadmap for High-Density PLD Designs
- 90% Cost Savings from APEX™ 20KE Derived from 75% Die Shrink
- Revolutionary MPLD Implementation Process Provides Guaranteed Functionality & Performance with Minimal Customer Involvement
- PLD/MPLD Solution Optimizes Product Life Cycle Management
- New Process: <15 Weeks From Design Start to Production!
MPLD Business Unit Mission Statement

- Provide Altera Customers with Easy, Fast & Risk Free Cost Reduction Path for High Density CPLDs
MPLD High Volume Solution

Density

High

Low

Volume

Low ↔ High

FLEX™10KE

APEX™

MPLD

ACEX™
Die Size Reduction

Original EP20K1500E

New MPLD 1500E Device

75% Reduction in Die Size
MPLD Opportunity

Unit Price ($)

Low ← Density → High

APEX 20KE

FLEX

ACEX

MPLD
Die Size, NRE & Unit Cost Comparison

- Large APEX PLD: 100% (Die Size)
- MPLD: 22% (Die Size)
- Standard Cell: 12% (Die Size)

NRE = Non-Recurring Engineering
## New MPLD Program Devices

<table>
<thead>
<tr>
<th>Device</th>
<th>APEX 20KE Die Size</th>
<th>MPLD Die</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP20K1500E</td>
<td><img src="image1.png" alt="Image" /></td>
<td><img src="image2.png" alt="Image" /></td>
</tr>
<tr>
<td>MP20K1000E</td>
<td><img src="image3.png" alt="Image" /></td>
<td><img src="image4.png" alt="Image" /></td>
</tr>
<tr>
<td>MP20K600E</td>
<td><img src="image5.png" alt="Image" /></td>
<td><img src="image6.png" alt="Image" /></td>
</tr>
<tr>
<td>MP20K400E</td>
<td><img src="image7.png" alt="Image" /></td>
<td><img src="image8.png" alt="Image" /></td>
</tr>
</tbody>
</table>
MPLD Process Description

- Complete Design Development in APEX 20KE Device
- 1:1 Mapping of Logic Elements & Embedded System Blocks
- Remove Configuration Circuitry & Multiplex Interconnect Overhead—Replace with Metal Routing
- Guaranteed Functionality & Performance
- Pin-to-Pin Compatibility
- Same Package Options as PLDs
MPLD Product Description

- 0.18-μ Process Technology—Same Process Technology as PLD
- Implementation Utilizes Common Base Die
- 5+ Metal Layers Dedicated to Customer Design
MPLD Implementation & Business Guidelines
**MPLD Engagement Flow**

**Step 1**
Customer Submits APEX 20K Netlist or Programmer Object File (.pof) & Required Paperwork

**Step 2**
Altera Reviews & Accepts Design

**Step 3**
Customer Provides Order for DCC & First Year Production Quantity with Schedule

**Step 4**
Altera Starts MPLD Implementation

**Step 5**
Altera Delivers Prototypes to Customer

**Step 6**
Customer Approves Prototype

**Step 7**
Altera Starts Production
MPLD Implementation Timeline

- Conversion & Testing: 2 to 3 Weeks
- Prototype Fabrication: 4 Weeks
- Prototype Signoff: 1 to 2 Weeks
- Production: 8 Weeks
- Total Duration: 15 to 16 Weeks
Testability & Verification Flow

1. Deliver POF File to Altera
2. Generate Netlist
3. Fix Test
4. ATPG
5. Place & Route
6. Timing Verification
7. Send Prototype to Customer
8. Volume Production
9. Customer Receives Prototype
10. Customer Approves Prototype

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Turn-Key Conversion Process

Deliver POF file to Altera

Customer Responsibility

Customer Receives Prototype

Customer Approves Prototype

Begin Conversion to MPLD

Altera Responsibility

Prototype Sent to Customer

Volume Production

Maintain Logic Placement

Extract Timing Data

Compare to PLD

Verify Functionality & Timing

Minimal Customer Effort

Deliver POF file to Altera

Customer Responsibility

Customer Receives Prototype

Customer Approves Prototype

Begin Conversion to MPLD

Altera Responsibility

Prototype Sent to Customer

Volume Production

Minimal Customer Effort
Recommended Design Guidelines

To Minimize Conversion Time
- Adhere to good synchronous design practice
- Minimize the number of global clocks
- Single global reset

Notification Is Requested for
- Gated clocks, clears or presets
- Inverted clocks
- Internally generated clocks

Altera Highly Discouraged the Use of
- Oscillator circuits
- Glitch generators
- Intentional delays
- Circuits with race hazards
Design Conversion Services

- DCC Charges Include:
  - ATPG Vector Generation
  - MPLD Place & Route
  - Tested Probe Card & DUT Board
  - Fabricate Masks
  - 10 Prototypes
Conversion Guidelines

- Availability of Fully Functional APEX Netlist, .pof File
- Compliance with Design Rules
- No Customization or Changes from Original Design
  - Strictly One-to-One Conversion
  - No Direct Conversion from Virtex or Other Competitor Devices
  - No N:1 Conversion
Test Methodology

- No Customer Involvement Required for Fully Compliant Designs
  - Fully Synchronous
  - No Feedback Loops/Non-Testable Nodes
- Test Vectors Generated Automatically Using ATPG
- Full Scan Will Be Introduced in MPLD Structure to Ensure Full Fault Coverage
- All Testability Issues Automatically Detected, and Corrected
For Each Generation, Only Highest-Density Members Are Offered as MPLDs
Porting to MPLDs

- **Altera Porting of PLD IP**
  - MegaCore™ Functions (PCI, DSP)
  - AMPP℠ Megafuntions

- **Porting of PLD Features**
  - EAB Memories in All Modes
  - JTAG BST Compliant with IEEE Std. 1149.1-1990
  - MultiVolt™ Circuitry
New MPLD Advantage

- **Low Cost**
  - Up to 89% Saving over APEX 20KE Devices

- **Fast Turnaround**
  - 4 to 5 Week Turnaround for Prototype

- **Low Risk**
  - Easy Conversion Process
  - Guaranteed Functionality & Timing Equivalence
## MPLD vs. Traditional ASIC Summary

<table>
<thead>
<tr>
<th></th>
<th>MPLD</th>
<th>ASIC</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Engineering Effort</strong></td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td><strong>Time to Market</strong></td>
<td>Best</td>
<td>Poor</td>
</tr>
<tr>
<td><strong>NRE Cost</strong></td>
<td>Average</td>
<td>Average</td>
</tr>
<tr>
<td><strong>Device Cost</strong></td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td><strong>Risk</strong></td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td><strong>Flexibility</strong></td>
<td>High</td>
<td>None</td>
</tr>
</tbody>
</table>
MPLD Summary

- Maximum Flexibility with PLD/MPLD Solution
  - Develop & Ramp into Production with PLDs
  - Migrate to High Volume with MPLDs

- Low Cost
  - Up to 90% Saving over APEX 20KE Devices
  - One Penny for 100 Gates

- Fast Turnaround
  - 4 to 5 Weeks for Prototypes
  - 8 to 9 Weeks for Production

- Easy “No-Risk” MPLD Implementation
  - Minimal Customer Interaction
  - Guaranteed Functionality & Performance
SoPC Design with Embedded Processors Solution
ARM & MIPS Hardcore Embedded Processors
Features

- 32 Bit RISC Processor Options
  - 200 MHz ARM922T™
  - 200 MHz MIPS32™ 4Kc™

- High Performance .18 µm 8LM TSMC Process

- AMBA™ Bus Architecture
  - Industry Standard Bus Architecture

- Stripe Memory
  - Single Port and Dual Port

- External Memory
  - SDRAM, DDRSRAM, FLASH, SRAM
Why Hard IP?

- True system on a programmable chip
  - Finally can integrate a fast CPU plus peripherals
- Embedded ASIC Contains Stripe Plus Custom Logic
  - Excalibur merges typical ASIC embedded processor logic with programmable logic
  - Software development begins immediately
  - Hardware/software co-verification is simplified over ASIC flow
  - Hard processor core runs at much higher frequency
  - Provides enhanced memory support
- Nios™ Soft Core Targets Lower Frequency Applications
  - Uses device logic resources
  - Easily migrate to next generation product
Block Diagram

- Embedded Processor Stripe
- DPRAM
- SRAM (Single Port)
- SDRAM Interface
- Flash Interface
- SDRAM Controller
- External Bus Interface
- Phase-Locked Loops
- ARM- or MIPS-Based Processor
- Dual-Port RAM Interface
- IP Blocks
  - Ethernet MAC
  - USB Device Controller
  - USB Host Controller
  - PCI Bus
- Master Port
- Slave Port
ARM Processor
**ARM922T Processor**

- Based on the ARM922™ (ARM920™ Derivative) and Incorporating the ARM9TDMI™
- High Speed Cache (8KB Instruction + 8KB Data)
- Single Cycle Repeat-rate SRAM and DPRAM
- MMU Facilitates the Implementation of Real-time Operating Systems (RTOS)
- 200MHz on Altera® 1P/8M, 0.18u Process at TSMC
- Advanced Built-in System Debug Features
Thumb: 16 bit instructions

A Subset of the 32-bit ARM® Instructions That Are Compressed Into 16-bits
- Processor core executes both 16 and 32 bit instructions
- Allows runtime inter-working between ARM and Thumb® code

Thumb Programs Typically
- Are ~30% smaller than ARM programs
- Are ~30% faster when accessing 16 bit memory
- Consume less power
- Require less external memory
MIPS Processor
MIPS32 4Kc Processor

- High-Performance MIPS® 32-bit RISC Processor
- Compatible with the MIPS32™ Architecture
- Supports User Level Code of R3000® and R4000® (32-bit mode)
- Memory Management Unit (MMU) For RTOS Support
- Harvard Cache Architecture With Separate 16 Kbyte Data Cache and Instruction Cache
- Single-cycle 16 x 16 Multiply Divide Unit
Internal Organization

- Multiply Divide Unit (MDU)
- Execution Core (ALU)
- System Coprocessor
- Memory Management Unit (MMU)
- Translation Lookaside Buffer (TLB)
- Instruction Cache (16 KBytes)
- Cache Controller
- Data Cache (16 KBytes)
- Bus Interface Unit (BIU)
- EJTAG
- Power Management
- AMBA Interface
# Hard Processor PLD Architecture

<table>
<thead>
<tr>
<th>Processor &amp; Interfaces</th>
<th>SRAM</th>
<th>SRAM</th>
<th>SRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARM</td>
<td>I-CACHE 8K Bytes</td>
<td>D-CACHE 8K Bytes</td>
<td>DPRAM</td>
</tr>
<tr>
<td>XA1</td>
<td>32 Kbytes SRAM</td>
<td>16 Kbytes DPRAM</td>
<td></td>
</tr>
<tr>
<td>XA4</td>
<td>128 Kbytes SRAM</td>
<td>64 Kbytes DPRAM</td>
<td></td>
</tr>
<tr>
<td>XA10</td>
<td>256 Kbytes SRAM</td>
<td>128 Kbytes DPRAM</td>
<td></td>
</tr>
</tbody>
</table>

- **Embedded Processor Stripe**
- **PLD**

- **ARM**
  - LEs: 4160
  - ESB Bytes: 6.5K
- **XA1**
  - LEs: 4160
  - ESB Bytes: 6.5K
- **XA4**
  - LEs: 16400
  - ESB Bytes: 26K
- **XA10**
  - LEs: 38400
  - ESB Bytes: 40K

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Stripe Layout

Stripe IP is placed physically on the top of the APEXE PLD
Excalibur Work Flow

Peripheral Pool
User Peripherals
Configure System

Hardware
Verilog / VHDL files
Quartus
User Design
Other IP

Software
C Header files
Peripheral drivers
Industry Standard Compiler/Linker/Relocator
User Code
Libraries
RTOS

Debugger + Trace Analyzer
Configuration
Executable
Trace
JTAG
Quartus Symbol

- Schematic Instantiation
  - Megafuctions>Embedded Logic>alt_exc_upcore
Excalibur MegaWizard

Select ARM®-Based or MIPS-Based™ Excalibur™

- Easily create the desired stripe configuration
MegaWizard

Select family and device

Hold processor in reset?

Boot from FLASH?

Endianess

Reserve pins

This page allows you to select and configure the Excalibur device to suite your particular application. It also allows you to enable or disable those ‘stripe’ modules that require external access and therefore pins to be reserved on the Excalibur device.

Select Excalibur family Excalibur_ARM
Select available device EPXA10

Reset operation

If the processor is held in reset, it can only be released by a write to the ‘stripe’ Boot control register by one of its two remaining bus masters.

Do you want the processor to be held in reset?

Do you want to Boot from FLASH?

Byte order

Little endian Big endian

Reserve pins

Do you want to reserve pins for any of the following ‘stripe’ modules?

- EBI (FLASH) Outputs Slow slew rate Inputs 3.3V LVTTL
- SDRAM Outputs Fast slew rate Inputs SSTL 2
- UART Outputs Slow slew rate Inputs 3.3V LVTTL
- Trace Outputs Fast slew rate No Inputs
# Clock Domains

<table>
<thead>
<tr>
<th>Name</th>
<th>Frequency (MHz)</th>
<th>Derivation</th>
<th>Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK_REF</td>
<td>10-66</td>
<td>Pin</td>
<td>Feeds Stripe PLL's and Fixed Frequency Logic (e.g. Watchdog Timer)</td>
</tr>
<tr>
<td>CLK_AHB1</td>
<td>&lt;=200</td>
<td>PLL1</td>
<td>Embedded Processor Bus</td>
</tr>
<tr>
<td>CLK_AHB2</td>
<td>&lt;=100</td>
<td>PLL1</td>
<td>Peripheral Bus</td>
</tr>
<tr>
<td>CLK_SDRAM</td>
<td>266</td>
<td>PLL2</td>
<td>SDRAM Memory Controller</td>
</tr>
<tr>
<td>SLAVE_HCLK</td>
<td>&lt;=100</td>
<td>PLD</td>
<td>Clocks the Slave Port of the PLD - Stripe Bridge; Invertible</td>
</tr>
<tr>
<td>MASTER_HCLK</td>
<td>&lt;=100</td>
<td>PLD</td>
<td>Clocks the Master Port of the Stripe - PLD Bridge; Invertible</td>
</tr>
<tr>
<td>CLK_PLDA[3..0]</td>
<td>&lt;=100</td>
<td>PLD</td>
<td>Clocks the PLD Application Interface (SRAM access); Invertible</td>
</tr>
</tbody>
</table>
Excalibur Clock Domains

Processor Domain
- PLL
- SRAM
- DPRAM
- Debug & Trace
- Processor + Cache + MMU
- Bridge
- AHB1 bus

AHB2 Domain
- PLL
- UART
- Timer
- SDRAM controller
- Bus Expansion

Typical PLD Domains
- DSP function
- Comms controller
- Bridge
- AHB bus

SDRAM Domain (133MHz)

PLL, Mul or Div
4 PLL’s in XA4 & XA10
2 PLL’s in XA1

USB
LCD
XXX

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On-Chip SRAM

- 2 Blocks of Independently-Addressable Single Port SRAM
  - Accessible to AHB Masters

- Up to 4 Blocks of Independently-Addressable Dual-Port SRAM
  - Accessible to AHB Masters
  - Accessible to PLD in Several Depth & Width Configurations
Efficient I/O Usage

- Certain Stripe Features Use Specific Pins
  - E.g. SDRAM Interface, Electronic Bus Interface (EBI), UART, Trace
  - These Pins Are Multiplexed
  - General-Purpose I/O If Not Used for Stripe

- ARM- & MIPS-Based Families Are Pin Compatible
Hard-Core Processor
Design Flow
SoPC System Design Work Flow

**Hardware**
- Peripheral Pool
- User Peripherals
- Verilog/VHDL Files
- Quartus™ Software
  - User Design
  - Other IP
- Configure System
- Generate
- Debugger & Trace Analyzer
  - Excalibur Solution
  - Trace
  - JTAG
- Native Core Developer Suite
  - User Code
  - Libraries
  - RTOS

**Software**
- C Header Files
- Peripheral Drivers
- User Code
- Libraries
- RTOS

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Design Flow

- **Software Design**: "C" Design
- **Hardware Design**: HDL
- **System Design**: HDL, Configuration Information (.sbd)
- **Software Tools**: "C" Netlist
- **Hardware Tools**: Hex Netlist
- **Quartus™ II Software (Fitting)**: Hex Programming Data

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Verification Flow

System Design

Software Design

“C”

Model Init

Hardware Design

Models

HDL

HDL

HDL

RTL Simulator

Software Tools

Hex

Configuration Information (.sbd)

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Key Design Software Support

- **SOPC Builder System Design Tool**
  - Interface to IP Blocks (Altera, Third-Party & Customer-Specific)

- **Integrated Design Environment**
  - Quartus II Software, Simulation Models, Synthesis Tools & Embedded Software Tool Chain

- **Debug & Trace Capabilities Speed System Debug & Development**
SOPC Builder

Configured Silicon Features

Configured IP Cores

Interconnect Ports

Completed SOPC Architecture
Soft Peripherals

- Flexible Bus Architecture Allows Integration of System Master & Slave Functions into PLD
- Altera Intellectual Property (IP) Functions Will Conform to Open Bus Interface Standard
- Altera IP Functions Will Include Hardware & Software Device Drivers
- APEX Architecture Offers High Capacity for Function Integration

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Hard IP</th>
<th>Soft IP</th>
<th>Size % XA/M4</th>
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<tbody>
<tr>
<td>UART</td>
<td>x</td>
<td>x</td>
<td>4%</td>
</tr>
<tr>
<td>Interrupt Controller</td>
<td>x</td>
<td>x</td>
<td>~2%</td>
</tr>
<tr>
<td>USB</td>
<td></td>
<td>x</td>
<td>15%</td>
</tr>
<tr>
<td>IrDA</td>
<td></td>
<td>x</td>
<td>5%</td>
</tr>
<tr>
<td>Ethernet 10/100 MAC</td>
<td>x</td>
<td></td>
<td>11%</td>
</tr>
<tr>
<td>Firewire</td>
<td></td>
<td>x</td>
<td>20%</td>
</tr>
<tr>
<td>PCI 64bit/66MHz</td>
<td></td>
<td>x</td>
<td>9%</td>
</tr>
<tr>
<td>Keyboard IF</td>
<td></td>
<td>x</td>
<td>~1%</td>
</tr>
<tr>
<td>LCD IF</td>
<td></td>
<td>x</td>
<td>~4%</td>
</tr>
<tr>
<td>DMA Controller</td>
<td></td>
<td>x</td>
<td>~8%</td>
</tr>
<tr>
<td>CAN</td>
<td></td>
<td>x</td>
<td>5%</td>
</tr>
<tr>
<td>IEEE1284</td>
<td></td>
<td>x</td>
<td>7%</td>
</tr>
<tr>
<td>IIC</td>
<td></td>
<td>x</td>
<td>1%</td>
</tr>
<tr>
<td>SDRAM Controller</td>
<td></td>
<td>x</td>
<td>5%</td>
</tr>
<tr>
<td>Timer/Counter</td>
<td></td>
<td>x</td>
<td>4%</td>
</tr>
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</table>
Models: Cornerstone of Verification

- **System Modelling**
  - Behavioural Modelling of Complete Hardware-Software System: “Co-Design”

- **System Verification**
  - Cycle Accurate Hardware Simulation Model
  - Based on Same RTL as Stripe Design

- **Module Level Verification**
  - Bus Functional Models Allow Simulation of Bus Interactions
Types of Simulation

- **Behavioral**
  - Algorithmic Level vs. Logic Gate Level
  - High Level of Abstraction
  - Bus Functional Model

- **RTL**
  - Data Flow Level
  - Code is Synthesizable
  - Excalibur Stripe Model

- **Gate Level**
  - Logic Gate Level
  - Low Level of Abstraction

- **Timing**
  - Gate Level with Timing Delay Information
Excalibur Based System

Excalibur Stripe

- Stripe-to-PLD (Master Port)
- PLD-to-Stripe (Slave Port)

SDRAM Model
- SDRAM Port

ROM Model
- EBI Port

SLD Logic

Slave
- Bus Functional Model Verification

Master
- Full Stripe Model Verification
Stripe Model

Complete Cycle Accurate Model of Embedded Stripe

- Processor
- Timer
- Interrupt Controller
- UART
- EBI
- DPRAM, SRAM
- SDRAM Controller
- AHB1-2 Bridge
- Stripe-to-PLD Bridge
- PLD-to-Stripe Bridge
- PLLs (limited model of behavior)
- PLD Configuration Not Modeled
Tool Flow

User Selections
Excalibur MegaWizard

Configured Stripe Instance
PLD Logic
3rd Party Synthesis

Top Level Design

Full Stripe Model
ModelSim/VCS
BFM

RTL
Behavioral

Gate-Level / Timing

Test bench
ROM model
SDRAM Model

C / Assembly Code
Netlist Output

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Simulation Procedure

1. Create Configured Stripe LPM
2. Generate Stripe Model Initialization Files (Optional)
3. Convert Code to ROM Model
4. Perform RTL Simulation
5. Synthesize PLD Logic
6. Place & Route in Quartus
7. Perform Timing Simulation
Boot Code

ROM Model represents FLASH

- Asm2rom Utility
  - Calls Arm Assembler, Linker and Converts Assembly Code
  - Puts <rom_image>.txt in Current Directory
  - Copies .txt to \simulation\modelsim Directory
  - User Editable Command File

- C2rom Utility
  - Calls ARM Compiler, Assembler, Linker and Converts C Code
  - Puts <rom_image>.txt in Current Directory
  - Copies .txt to \simulation\modelsim Directory Stripe Initialized
  - User Editable Command File
Discussion for SDR with Altera Solutions
What is Software Defined Radio (SDR)?

“Software Defined Radio (SDR) is a collection of hardware and software technologies that enable reconfigurable system architectures for wireless networks and user terminals.”

FAQ from www.sdrforum.org
Advantage of SDR

Ideally beneficial for each group

1. Service Provider/System Development Company
   - Unified service for different type of technology
   - Easy upgrade of Terminal/System
2. User
   - Unconscious of different system
   - Unified Terminal
What is the Hardware Part for SDR

**Baseband**

1. Muti-mode modem
   AMPS/CDMA Phone
2. Reconfigurable Modem
   Soft Hardware Platform

**Digital IF**

1. Simple Digital IF
   Digital Up/Down Converter
2. Complex Digital IF
   Channelizer/Dechannelizer
   Multi Band

**ADC/DAC**

1. ADC
   Wide-Band, High Resolution, Low power
2. DAC
   High-Speed, High Resolution, Linearity
Basic Structure of SDR

- **Digital**
  - User
  - Baseband (Modem, FEC, Mux/Demux, Codec, Interface etc)
  - Processor
  - Digital IF

- **Analog**
  - ADC
  - DAC
  - RF

**ALERTA**
Baseband
### How can it be realized? - Simple Example

#### Assumptions
- Multiple protocol in a single solution
- We assume GSM, IS-95, cdma2000, UMTS
- We assume each has 1M gates.

<table>
<thead>
<tr>
<th></th>
<th><strong>ASIC</strong></th>
<th><strong>PLD</strong></th>
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</thead>
<tbody>
<tr>
<td>Typical gate</td>
<td>4M gates/Hardwire</td>
<td>1M gates : Programmable</td>
</tr>
<tr>
<td>Price</td>
<td>Low</td>
<td>can be low</td>
</tr>
<tr>
<td>Flexibiliy</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>NRE</td>
<td>Very very high</td>
<td>No</td>
</tr>
<tr>
<td>Iteration</td>
<td>Months</td>
<td>On-the-fly</td>
</tr>
<tr>
<td>Power</td>
<td>Low</td>
<td>can be low</td>
</tr>
<tr>
<td>Performance</td>
<td>Accomplished</td>
<td>Accomplished</td>
</tr>
</tbody>
</table>
Baseband Implementation

Alterra Platform

- Multiple protocol with ONE pair of platform and memory!!
- Handset can be configured via common broadcasting channel
What’s Altera Advantage for baseband?

• **Embedded Processor**: ARM, MIPS
• **Density Leadership**: Up to 1.5M gate/600Kbit Mem. available today
  3M gate/1.1Mbit Mem. available within 6 months
• **Performance**: 1.5um technology + all copper layer interconnection
  + higher number of metal layer for fast/efficient routing
• **Price Leadership**: Redundancy Technology + 12” wafer technology
  -> Higher Yield, Lower price
• **Power Consumption Leadership**: 1.5V core voltage
• **High Speed I/O Leadership**: Various kind of High Speed I/O
• **Package Leadership**: FlipChip™ Technology
• **And more features ...!!**
Digital IF
How can it be realized? - Simple Example

- Digital IF
  - Require Very Accurate Clock - PLL
    In the receiving end, clock jitter causes signal degradation
  - Must use Digital Filters - FIR Compiler
    Coefficient generator, Various Filter type,
    Serial/parallel implementation, Poly-phase etc
  - Must use NCO - NCO Compiler
    Modulation, DDS etc
  - Must use Arithmetic - LPM
    Multiplier, Adder etc
  - You Think, Altera will realize it.
Digital Approach is good because...

• We can reduce the number of ADC/DAC
• We can remove I/Q asymmetry
• We can suppress Analog noise
• We can build very sharp filter efficiently
• We can change the configuration easily
Digital Down Conversion

- Chose IF that can be handled by ADC
- Bandpass sampling
- Shift to the Baseband
- Select Desired Spectrum
Design Consideration

- What’s the appropriate sampling frequency of ADC?
- What’s the appropriate resolution of ADC?
- What’s the dynamic range of ADC?
- What’s the reference clock rate for NCO?
- What’s the output frequency of NCO?
- What’s the performance of Multiplier?
- What’s the structure of FIR?
- What’s the input resolution of FIR?
- What’s the resolution of coefficient?
- What’s the output resolution of FIR?
QPSK Modulator: Reference Example
BPSK Modulator: Reference Design

1FIR(Serial), 1NCO

APEX20KC Target

- Processing status: Fitting Successful
- Timing requirements/analysis status: No requirements
- Chip name: fitlertest
- Device name: EP20K100CT144C7
- Total logic elements: 1407 / 4160 (33%)
- Total pins: 13 / 92 (142%)
- Total ESB bits: 2304 / 53248 (4%)
- Fmax = 91.19MHz

Mercury Target

- Processing status: Fitting Successful
- Timing requirements/analysis status: No requirements
- Chip name: fitlertest
- Device name: EP1M120F484C5ES
- Total logic elements: 1347 / 4800 (28%)
- Total pins: 13 / 303 (4%)
- Total ESB bits: 2304 / 49152 (4%)
- Fmax = 175.59MHz
BPSK Modulator: Spectrum Capture
What’s Altera Advantage for Digital IF?

- **Flexibility**: Standard + User functions + Integration
- **Performance**: Core Performance increases dramatically
  - New architecture of LE
  - Multiple level of interconnect
  - Technology (Full CU layer, Thin line width etc)
- **PLL**: Provide accurate clock for ADC/DAC
- **IP**: Easy-to-use FIR compiler, NCO compiler
  -> Realize what you think in a few minutes
- **Power Consumption Leadership**: 1.5V core voltage
- **Price**: HardCopy™ for moderate range of quantity
- **High Speed I/O**: Eliminate Board-to-Board High Speed I/O Buffer
Examples
Application Example - BTS

Control (CPU) I/F

Control/Interface with BSC

1FA (Alpha, Beta, Gamma Sectors)

Modem
Modem
Modem
Modem

CPU

PLD
PLD

A/D

DDC(I/Q), Filtering Demuxing

Adding Filtering, DUC(I/Q)

A/D

D/A

Attenuator

HPA

LNA

IF/RF/Antenna

Modem
Modem

Atten

LVDS

LVDS

LVDS

ALTEGRA
Application Example - BTS (Cont’d)

- Adder + High Speed Serial I/O
- Modem output (Ex.): 1.2288Mcps x 2X filtering x 3 sectors x I/Q x 2 Antennas x 10 bit resolution = 294.912Mbps serial data
- So, ChipX32 clock will be reference clock and operate CDR or LVDS with 10X Mode (Mercury or APEX-II)
- Adder is easily implemented using LPM

- High Speed I/O
- Medium Density
- High Performance
- DSP functions
- PLL
Application Example - BTS(Cont’d)

Mercury
+ CDR Buffer
+ APEX

Full APEX-II Implementation
Application Example - Channelizer/Dechannelizer

Channelizer: CDMA2000

APEX, APEX-II, Mercury
Application Example - Channelizer/Dechannelizer

Dechannelizer: CDMA2000

- ADC
- PLL
- NCO1
- NCO2
- NCO3
- FIR
- Mux

LVDS
- CDR

APEX, APEX-II, Mercury
Altera; Aims the future

- Altera is being changed? -> Definitely YES!
- How?
  - Intensive Efforts on IP: More and more IP-lized
  - Easier way to design: Project on a single device
  - Really Suitable Silicon Solution
    Density, Power, Price, Unique features
  - Leading or up-to-date solution
    Approaching ASIC Replacement: Cost, density, power
    More professional solution provider
    Concept-to-silicon philosophy
- Should not be SIMPLE PLD SUPPLIER!
How can it be realized? - Simple Example

- System on a programmable chip?

  - Require Larger Device - This is our fundamental goal
  - Require Cost Down - dramatically decrease annually
  - Require Various Functions
    Processor? ARM, MIPS, NIOS
    Memory? More integrated memory
    Peripheral? UART, Memory controllers, Interrupt handle
    Interface? PCI, UTOPIA, USB etc
    Professional? FEC, Ethernet MAC, ATM, SONET, SDH etc
    High Speed I/O? LVDS, CDR, LVPECL etc
  - And more.. Customers are the standard.