FPGA Co-Processing for DSP
Agenda

- Applications of FPGA-Based Co-Processors for DSP
- Development Tools & Methodologies Available from Altera to Build Co-Processors
  - SOPC Builder
  - DSP Builder
- FPGA Co-Processor Development Examples
  - QAM Modulator
  - FIR Filter
Growing Demand for MIPS & Memory Bandwidth

- Growth Drivers
  - Algorithm Complexity
  - Security
  - Multiple Users

Digital Signal Processing (DSP) MIPS & Memory Bandwidth vs. Time

Application Requirements

Digital Signal Processors

20 YEARS of ALTERA INNOVATION
Co-Processing on FPGAs

Processor on FPGA

Processor External to FPGA
When Do FPGA Co-Processors Reduce System Cost?

- Off-Loading Algorithms to Co-Processor Reduces Number or Cost of Digital Signal Processors

Applications
- Algorithms with Large Amount of Digital Signal Processing & Small Amount of Control Processing
FPGA Co-Processor Applications

- **Wireless**
  - 2.5-G EDGE Equalization
  - 3-G Baseband Processing
    - HSDPA
    - 1xEVDV
  - 3-G RF Linearization

- **Consumer**
  - Broadcast - Studio & Cable Plant
  - Digital Entertainment – MPEG2 & MPEG4

- **Medical**
  - Imaging

- **Wireline Communications**
  - Encryption
  - Framer
  - Traffic Management
  - TCP/IP

- **Computer & Storage**
  - Data Analysis & Routing Engine
  - Digital Imaging

- **Military & Aerospace**

- **Security**
DSP Development
Tools & Design
Methodology
FPGA Co-Processor Design Tools

**SOPC Builder**
- Embedded Processor
- Memory
- Stand-Alone Processor

**DSP Builder**
- Embedded Processor
- IQ Map
- NCO
- Processor + Co-Processor

**Dedicated Hardware Architecture**
- IQ Map
- NCO
- FIR
- Dedicated Hardware Architecture

**Tools**
- DSP Builder
- SOPC Builder
DSP Builder Overview

DSP Builder

- Creates HDL Code
- Creates Simulation Test Bench
- Creates Processor Plug-In
- Download Design to Development Board
- Verify in Hardware

HDL Synthesis

Model Technology

Model Technology

Synthetic

SignalTap® II

QUARTUS® II

SOPC Builder

MATLAB® & SIMULINK®
DSP Builder Library Components

- Arithmetic
- Bus Manipulation
- Complex Signals
- Logical Components
- SOPC Ports
- Storage
- MegaCore® IP
- Rate Change
- State Machine
- Altera Library
- DSP Board
MegaCore IP in DSP Builder

DSP Builder MegaCore® Functions
- FIR
- FFT
- Viterbi
- Turbo
- Reed Solomon
- NCO
DSP Builder Support for Multiple Clock Domains

- Inherit Sampling Frequency (FS)
- Adhere to Clock Design Rules
- All Sample Times Match One of Phase-Locked Loops (PLLs) Output Clock Periods
- Simplify Analysis & Implementation of Multi-Rate System
  - Up Sampling
  - Down Sampling
State Machine Builder

FIFO Example

State Machine Builder v2.1.0

Current State | Condition           | Next State       |
--------------|---------------------|------------------|
empty         | (push=1) && (count_in=250) | push_not_full    |
empty         | (push=0) && (pop=0)    | idle             |
full          | (push=0) && (pop=0)    | idle             |
full          | (pop=1)               | pop_not_emp      |
idle          | (pop=1) && (count_in=0)| empty            |
idle          | push=1                | push_not_full    |
idle          | (pop=1) && (count_in=0)| pop_not_emp      |
idle          | (push=1) && (count_in=250) | full      |

Inputs | States | Conditional Statements | Design Rule Check |
--------|--------|------------------------|------------------|
Add     | Change | Delete                 | Move Up          |
| Move Down | OK     | Help                   | Cancel           |
Sub-System Builder

- Import Existing VHDL Design into Simulink
- Simulink Simulation Options
  - Convert into DSP Builder Blocks or MATLAB Functions
  - Treat VHDL Design as Black Box
Signal Compiler

- Generates VHDL Design Files
- Generates Tool Command Language (Tcl) Scripts
- Generates Testbench
- Enables Parameterization of IP Blocks
- Launch Hardware Compilation from Simulink Cockpit
Stratix DSP Development Board

- 80-Pin I/O Connector
- Altera® Nios® Expansion Prototype Connector
- Prototyping Area
- Push-Button Switches
- 9-Pin RS232 Connector
- 40-Pin Connector for Analog Devices Evaluation Boards
- LEDs
- Texas Instruments Connectors Can Be Found on Underside of Board

- 14-Bit, 165-MHz D/A
- 12-Bit, 125-MHz A/D
- SMA Connector
- 5-V Power Supply
Altera DSP Development Kits

Contains Everything You Need to Develop High-Performance DSP Designs on FPGAs
QAM Modulator Co-Processor Design Example
Modem Reference Design

- Installed with Code Composer Studio As a Tutorial
  - `C:\ti\tutorial\dsk6711\modem`
- Used to Demonstrate CCS Functionality
- 16 QAM TX Modem
<table>
<thead>
<tr>
<th>Functions</th>
<th>Code Size</th>
<th>Count</th>
<th>Incl Total</th>
<th>Incl Maximum</th>
<th>Incl Minimum</th>
<th>Incl Average</th>
<th>Excl Total</th>
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<td>341493</td>
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<td>493</td>
<td>540</td>
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<td>723</td>
<td>716</td>
<td>721</td>
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Modem Design Hardware/Software Petition

Main 100%

Initialize 3%
Add Noise Signal 0.5%

Modem Transmitter 96.5%

Hardware Accelerator
- Shaping Filter 82%
- Modulation 8%
- Sine Lookup 2.5%
- Cosine Lookup 2.5%
Modulator Co-Processor

DSP Builder Used to Build Hardware DSP Data Path
Avalon™ Interface in SOPC Builder
DSP Builder— SOPC Builder Import

Import DSP Builder Generated Co-Processor into SOPC Builder
SOPC Builder Integration

Modem Co-Processor (fir_comp) Integrated with TI EMIF I/F (TIMaster)
FIR Filter Co-Processor Design Example
Driving Down System Costs

**Multi-Processing**

DSP

**Digital Signal Processor + FPGA Co-Processor**

DSP

FPGA

FIR

Memory

SOPC World 2003

20 Years of Altera Innovation
FIR Co-Processor Design Example

- FIR Parameters
  - 128-Tap
  - 16-Bit Data, 14-Bit Coefficients

- Four FIR Implementations for Comparison
  - TI C6711-Optimized TI DSPLib Function
  - TI C6416-Optimized TI DSPLib Function
  - Altera Eight-Cycle FIR Co-Processor
  - Altera One-Cycle FIR Co-Processor
**TI Filtering Library (DSP Lib)**

- C-Callable Optimized Assembly Routines
- TI C67x DSPLib: Fir Filter (Radix 8)
  - Formula: \( Nh \times Nr /2 + 13 \)
    - \( Nh \) = Number of Coefficients
    - \( Nr \) = Number of Samples
  - \(~1\) Sample/ 64 Cycles (128 Tap Filter)
- TI C64x DSPLib: FIR Filter (Radix 8)
  - Formula: \( Nh \times Nr /4 + 17 \)
  - \(~1\) Sample/ 32 Cycles (128 Tap Filter)
Filter Co-Processor Design Example

- Current Implementation
  - 100 MHz, 32-Bit, Asynchronous EMIF on DSK
  - TI Writes 300 Samples to Co-Processor (Input Data)
  - Filter & Send Output to TI
<table>
<thead>
<tr>
<th>Device</th>
<th>Solution</th>
<th>FIR Performance (MHz)</th>
<th>Device Cost****</th>
<th>Cost per FIR MHz</th>
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<td>TI C6713-200</td>
<td>64-Cycles**</td>
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<td>1-Cycle***</td>
<td>170</td>
<td>$84</td>
<td>$0.49</td>
</tr>
</tbody>
</table>

* FIR 128 Tap, 16-Bit Data, 14-Bit Coefficients
** DSPLib Optimized Assembly Libraries from Texas Instruments
*** Optimized MegaCore FIR Compiler from Altera
**** Pricing in Quantity of 100 at Arrow 6/25/03
14X Reduction in System Costs

<table>
<thead>
<tr>
<th>Architecture</th>
<th>FIR Performance (MHz)</th>
<th>Total FIR Performance (MHz)</th>
<th>Device Costs</th>
<th>Total Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>9 * TI C6416-600</td>
<td>9 * 18.75</td>
<td>167</td>
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<td>$1,440</td>
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<tr>
<td>Altera EP1C12-8 + 1 TI c6713-200</td>
<td>170 + 3</td>
<td>173</td>
<td>$84 + $25</td>
<td>$110</td>
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</tbody>
</table>
FPGA Co-Processors for DSP Offer Many Advantages

− 10X Performance Boost
  ● More Channels
  ● More Complex Algorithms
  ● Increased System Throughput

− 10X Cost Reduction
  ● Fewer Components

− Complementary to DSP-Based Systems
  ● Offloads Existing DSP
  ● Integrates Into Existing DSP IDE
  ● Evolution Not Revolution
Altera Code: DSP Solutions

- FPGAs
  - Stratix, Stratix GX, Cyclone

- Development Tools
  - DSP Builder, SOPC Builder

- Intellectual Property
  - FIR, FFT, Viterbi, Turbo, Reed Solomon, NCO
  - AMPP Third-Party Partners

- Development Kits
  - Altera
    - Third-Parties

- Design Services
  - ACAP Third-Party Partners

- Training
20 YEARS of ALTERA INNOVATION

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