

20 YEARS of

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INNOVATION



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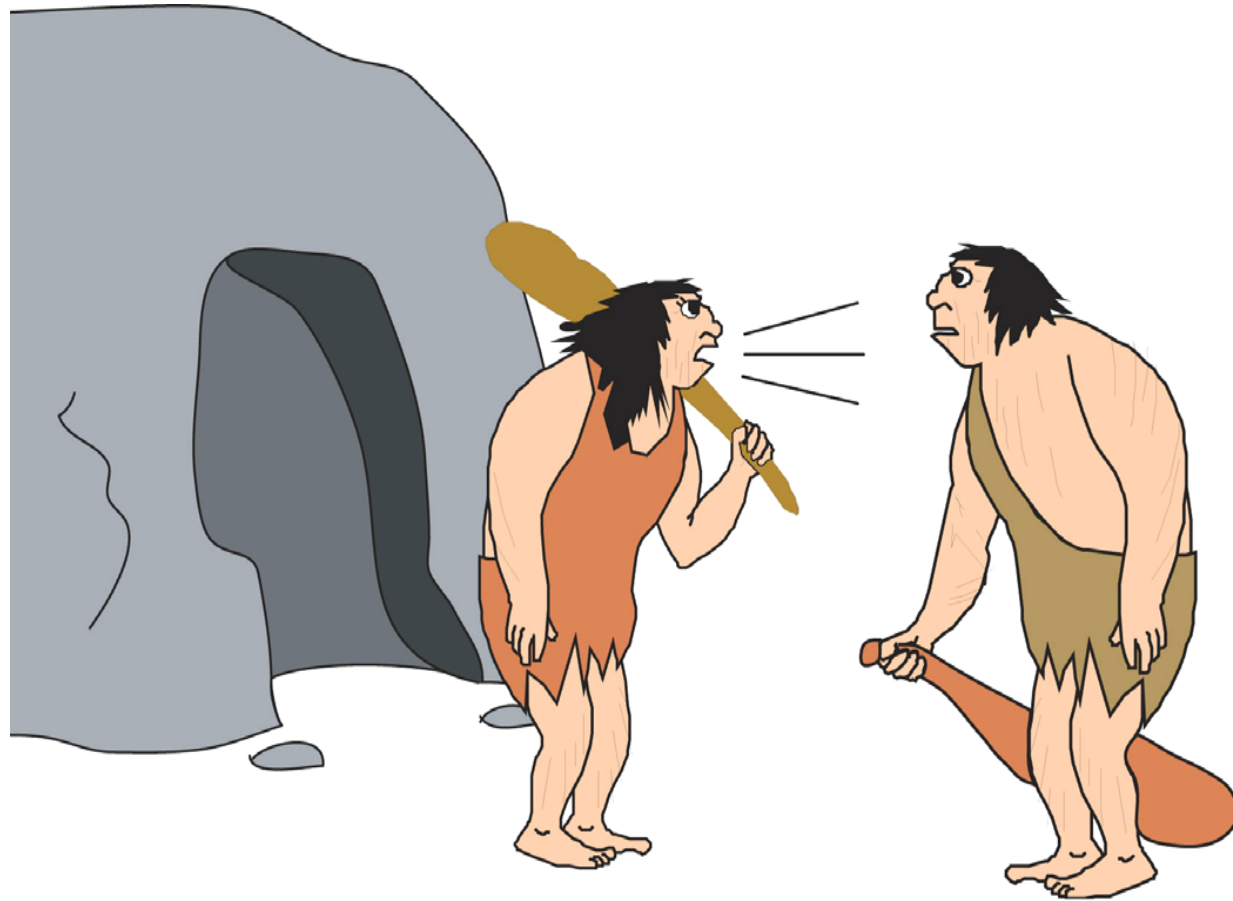
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# Solutions for Designing High-Speed Systems

# Agenda

- Evolution of Data Communications
- Data Integrity Challenges
- Signal Integrity & Board Design Challenges

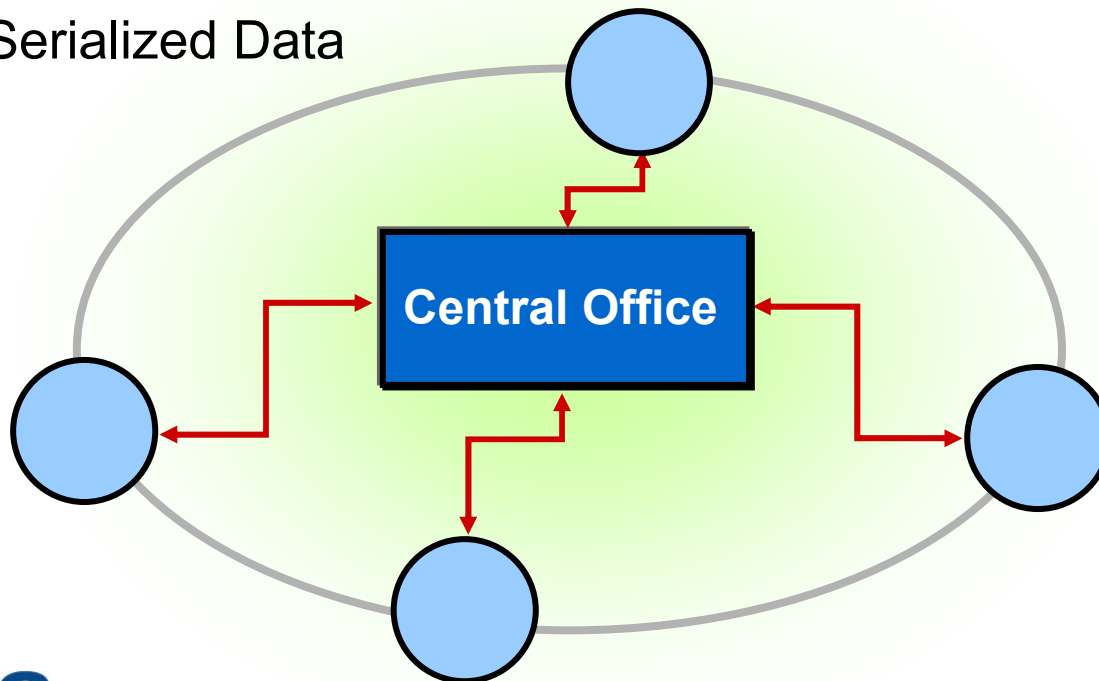
# History of Communications



# History of Communications

## ■ More Efficient Networks

- Dramatically Reduces Number of Point-to-Point Connections
  - Central Office
  - Serialized Data



# Evolution of Data Transfer

- Faster Networks → More Problems to Solve
- Two Main Problems
  - Data Integrity
  - Signal Integrity
- Need for Added Complexity & Intelligence

# Datacom Standards

- Evolution of Datacom Standards
  - ATM, Ethernet
- Ethernet: the Choice for 70% of Data Networks
  - First Developed in 1973 by DEC, Intel & Xerox
  - 10Base-T: 10 Mbps
  - 100Base-T: 100 Mbps (Fast Ethernet)
  - 1000Base-T: 1 Gbps (Gig-E)
- Gigabit Ethernet: Uses 4 Pairs of Twisted Pair at 250 Mbps
- 10 Gigabit Ethernet (XAUI): Uses 4 Pairs at 3.125 Gbps

# Why Serial Data? Why Everywhere?

- Parallel Data Worked for Short Distances & Low Clock Rates
  - Skew & Timing Budget
  - Signal Count, Power, Connector Size, Pin Count, EMC Issues
- PCB Real Estate (Can't Just Go Wider)
- Parallel Data Buses Are EXPENSIVE!!
- Serialization Solves Most of These Problems



# Trends

## Communication

The diagram illustrates the evolution of communication standards. Arrows point from the labels 'Communication', 'Computers', and 'Industrial' to their respective standards in the table below.

	PCI	PCI Express	Parallel RapidIO	Serial RapidIO
I/O Standard	33 Mbps	2.5 Gbps	800 Mbps	3.125 Gbps
Total Reach	7 cm	50 cm		
Data Channels	32	4 Differential		
Clock Channels	1	0		
Control Channels	4	0		
Total Pins/Pair	74	16		

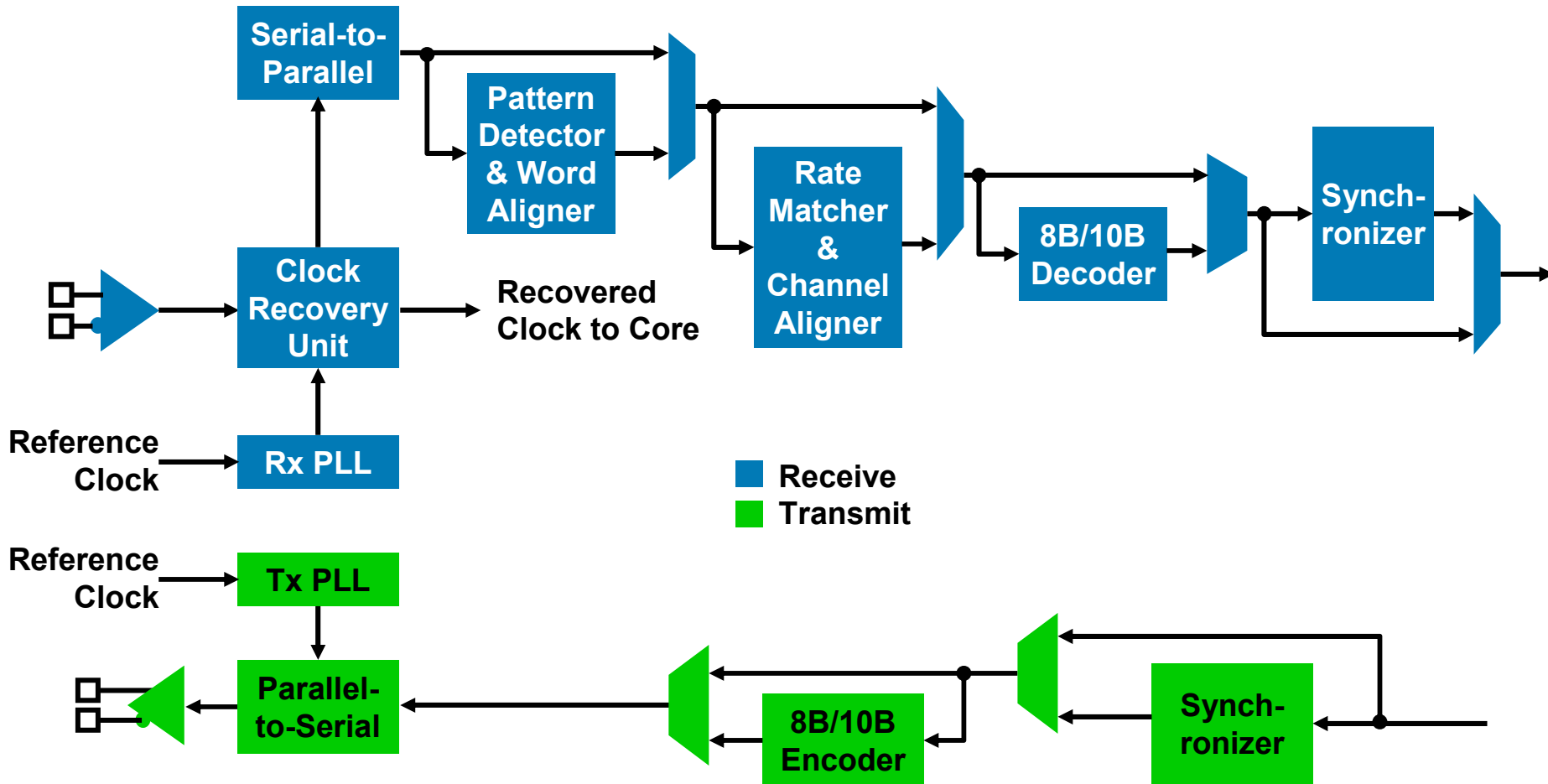
# Data Integrity

- Added Overhead in the Data Stream
  - Clock & Data Recovery
  - Initialization of the Link
  - Data Encoding/Decoding
  - Word Boundary
  - Skew Compensation, Clock Domain Decoupling
  - Error Checking/Recovery
- Consider XAUI

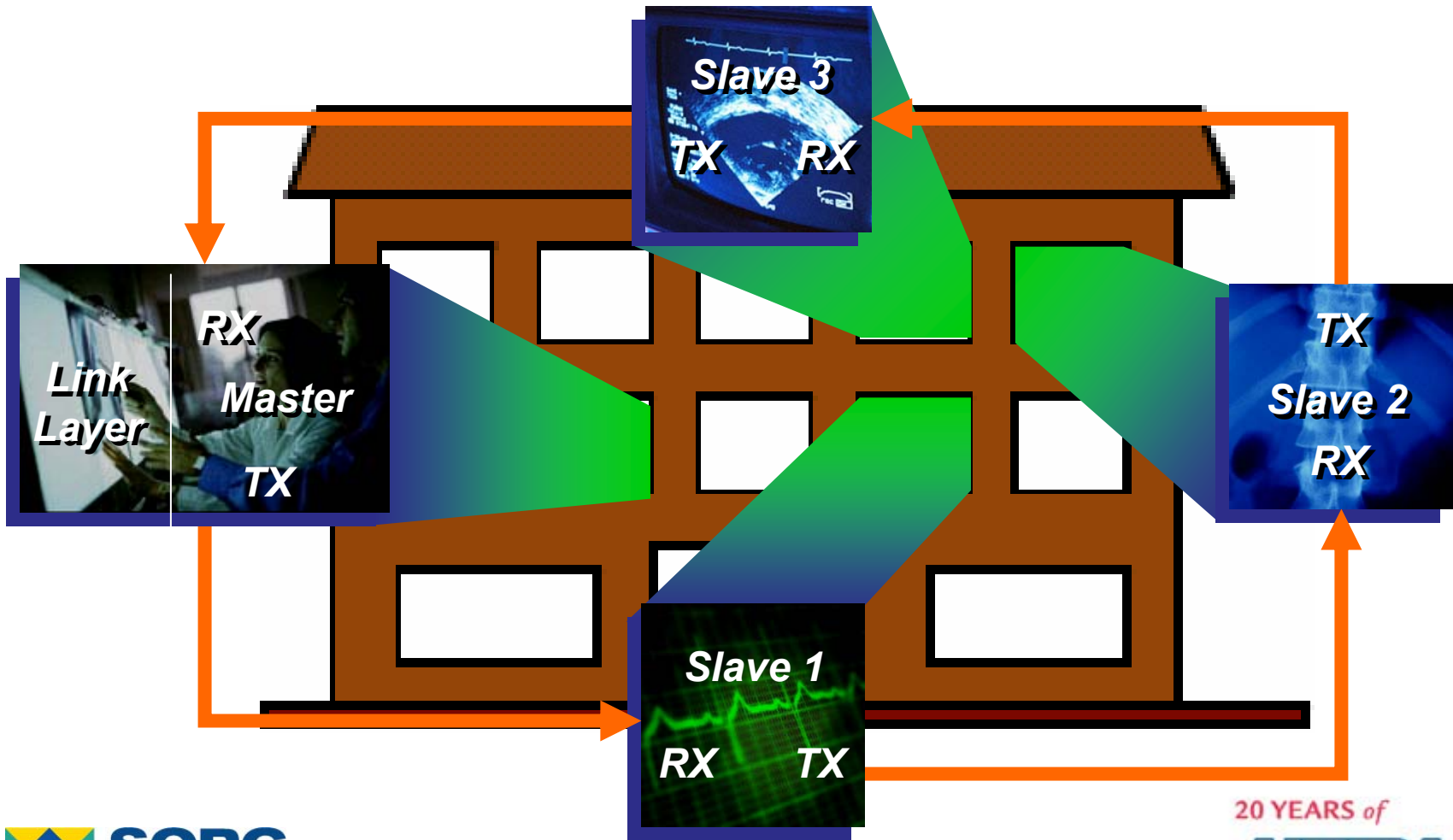
# XAUI Data Management

- Encode XGMII into 10 Bits/Lane At 3.125 Gbps
- Synchronization of Code Groups on Each Lane
  - Word Alignment ||K||
- Deskew of Received Code Groups across Lanes
  - Channel Aligner ||A||
- Clock Decoupling Across Domains
  - Rate Matching ||R||
- Conversion of XGMII Idle Control Characters to a Random Sequence of XAUI Control Characters

# XAUI Implementation in Stratix GX



# Case Study 1: Medical Instrumentation



# Case Study 1: Medical Instrumentation

- Network of Medical Instruments in a Building
  - Master Slave Configuration, Ring Structure
  - Slave Instruments Transfer Data to Master Analysis Center
  - Data Transfer at 3.125 Gbps
  - 2 Redundant Channels

# Case Study 1: Requirements

- Data Flows in One Direction
- Simple Flow Control & Initialization
  - Asynchronous System
  - Not Too Concerned about Dropped Packets
- Initialization
  - Master Sends Beacon Containing Address of Slave of Interest + `||XXXXXX||`
  - Once Link Initializes, Data Transfer Starts
  - Re-Initialize in Event of Failure

# Case Study 1: Implementation

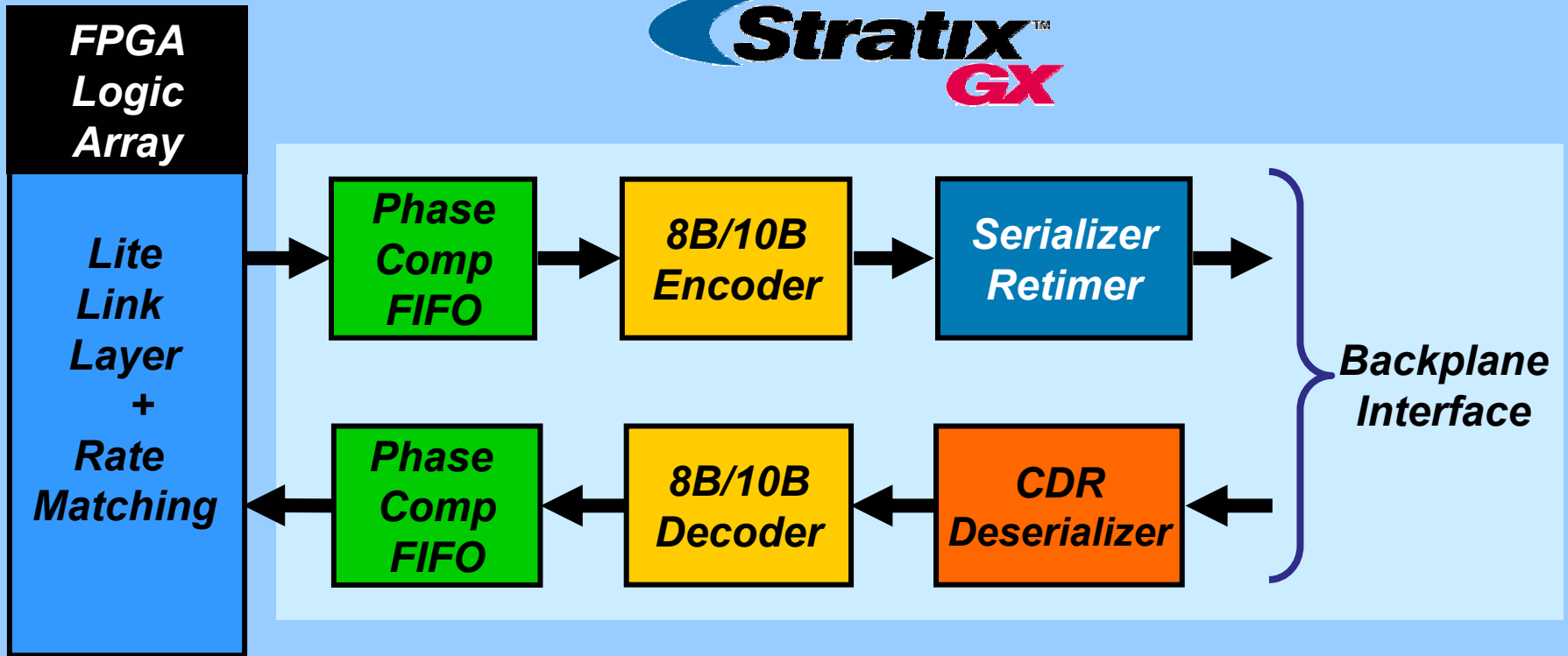
- Utilizes Stratix™ GX Device's Built-In XAUI Hard IP
  - Word Align, Channel Align, Rate Match, 8B10B Coding & Phase Compensation FIFO
- Use of a Simple Protocol
- Link Layer Implemented in the FPGA Logic Array of Master Node
- Non XAUI Network, But Uses the Built-in XAUI Hard IP



# Case Study 2: Semiconductor Test Equipment

- Point-to-Point Communication
  - 2.5 Gbps Serial Data Rate across Backplane
  - Efficient Data Transfer: Low Latency, Low Overhead
  - Does Not Need Quad-Based Data Transfer
  - Cannot Use A Heavy Protocol

# Case Study 2 : Implementation



# Case Study 2: Implementation

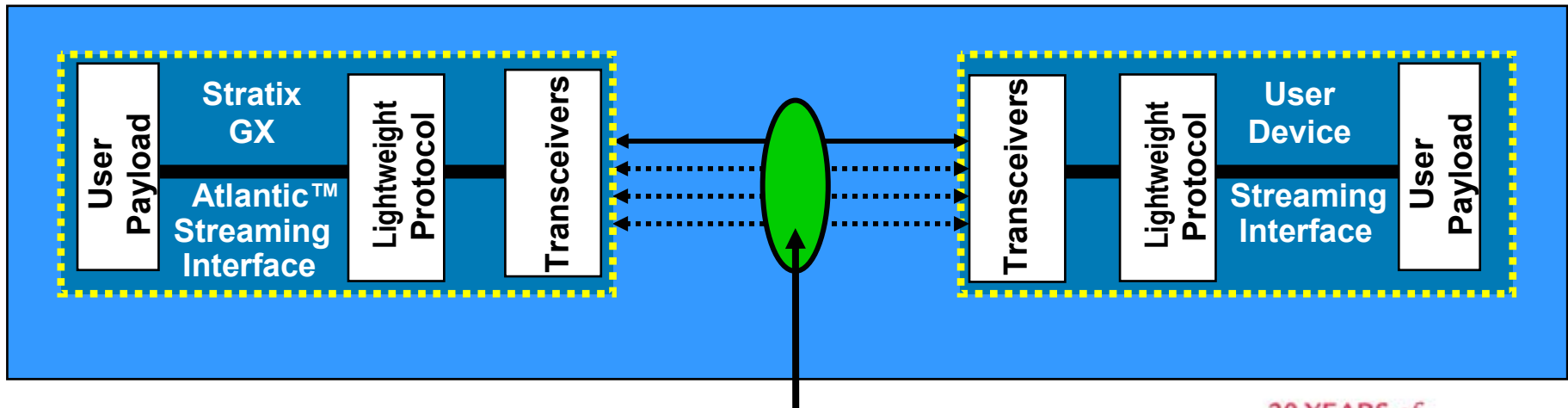
- Most of the XAUI Hard IP Not Necessary or Applicable
  - Rate Matching Implemented in the FPGA Logic Array
- Light Link Layer Incorporated in FPGA Logic Array
  - Cut-through Mode, CRC, Error Recovery
- Leverages Flexibility of FPGA Solution!

# XAUI Protocol

- XAUI : 4 Lanes of Traffic → Overhead
  - Synchronization
  - Channel to Channel Skew
  - Rate Matching
  - Initialization
- Very Heavy Protocol (Lots of LEs)

# Simple Serial Link Applications

- Packet or Streaming Data
- Chip-to-Chip Connectivity
- Board-to-Board Connectivity
- Shelf-to-Shelf Connectivity
- Backplane Communication
- Optical Connectivity



One or More Channels

# SerialLite Protocol

- A Very 'Lite' Protocol
- Highly Configurable
- Logic Element (LE) Usage Based on Complexity

***Optimal for Most Systems***

***NOT Requiring Protocol Standard Compliance  
(i.e., Interoperability to Existing Protocol)***

# SerialLite Features

- 1 - 16 Bonded Lanes
- 622 Mbps - 3.125 Gbps per Lane
- Low Logic Usage, Protocol Overhead & Latency
- 16-Bit to 128-Bit Programmable Atlantic Interface
- Data & Nested Priority Packets
- Error Detection on All Packets & Optional CRC

# SerialLite Protocol

- Availability
  - Single Lane Version: December 2003
  - Multi-Lane Complete Package: May 2004
- Open Standard: Freely Available for Everybody to Use
- Specification Available Today, Contact Altera Sales Representative for Details

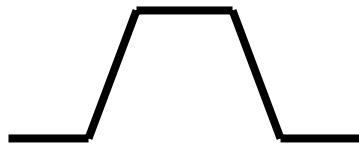




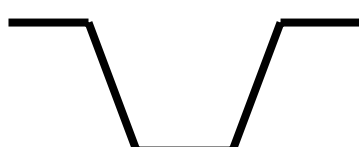
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# Signal Integrity

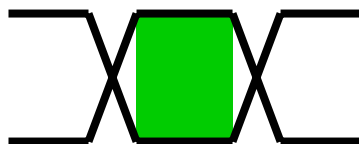
# Eye Diagram



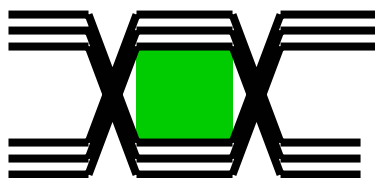
Waveform Represents a Logical '1'



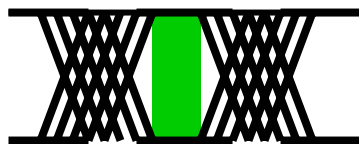
Waveform Represents a Logical '0'



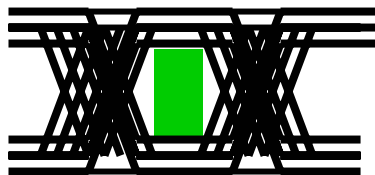
Ideal Eye Diagram with No Noise



Eye Diagram with Voltage Noise



Eye Diagram with Timing Noise



Eye Diagram with Voltage & Timing Noise

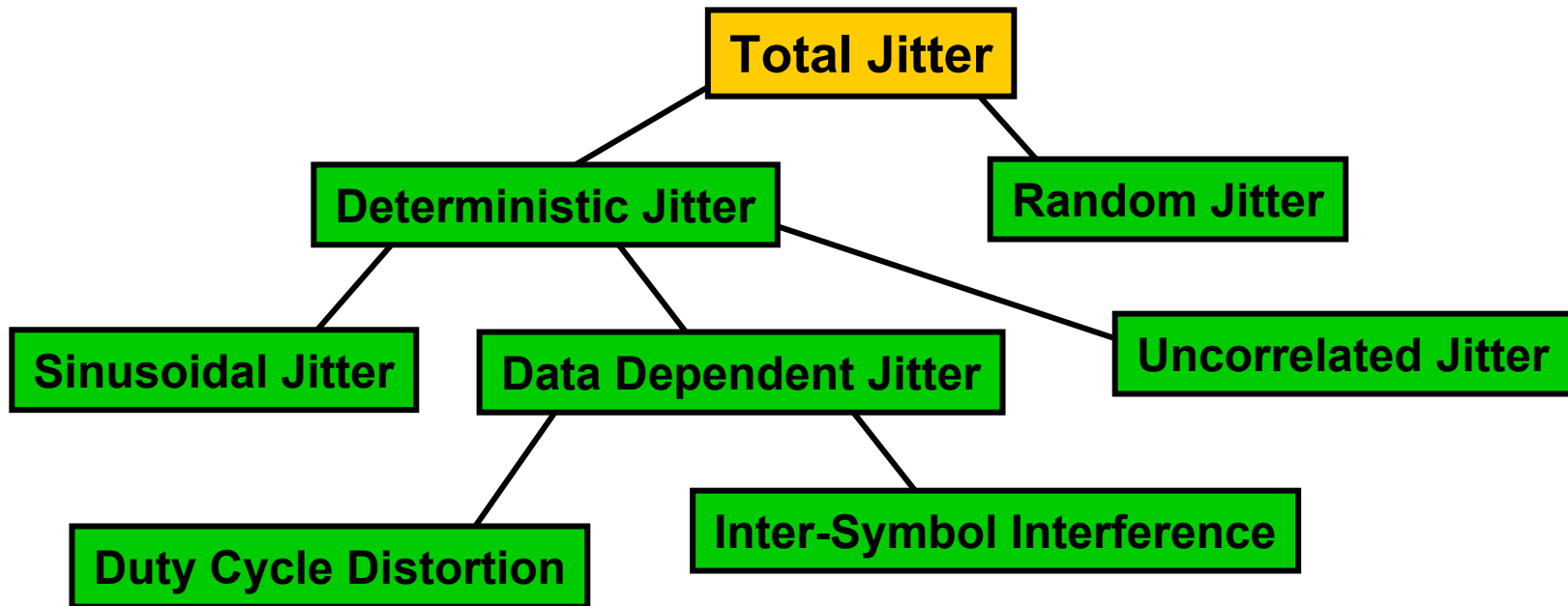
# Signal Integrity

- Bottom Line: Jitter = BAD!
- “Deviation from Ideal Timing of An Event”
- Sub-Optimal Board Design Degrades Otherwise Clean Data
- Some Common Issues
  - Bad Transmission Medium
  - Power Supply Integrity
  - Cross Talk
  - SSO Noise

# Jitter Components

- Two Kinds of Jitter
  - Deterministic & Random

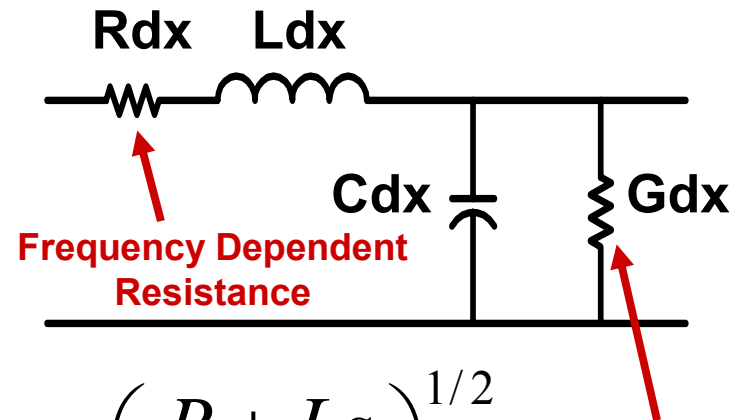
## *Total Jitter Constituents*



# Board Losses

- Skin Effect Causes Frequency Dependent Series Resistance on the Line
- Dielectric Absorption Causes Conductance of the Line to Vary with Frequency
- Both the Skin Effect & Dielectric Absorption Will Increase Attenuation At Higher Frequencies

## Lossy Model



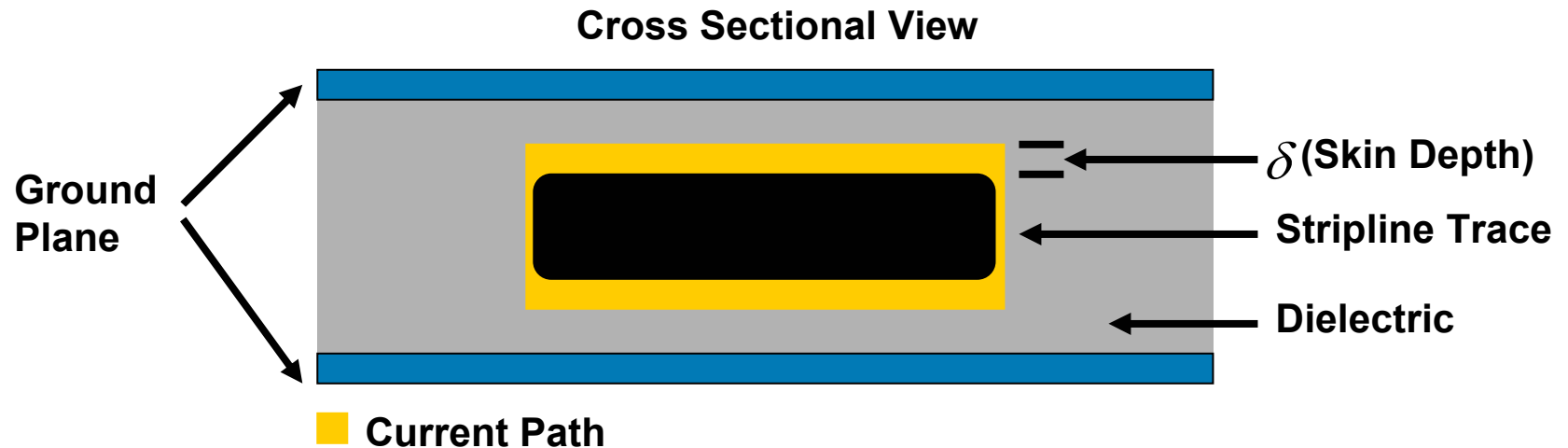
$$Z_0 = \left( \frac{R + Ls}{G + Cs} \right)^{1/2}$$

Frequency Dependent Resistance

Frequency Dependent Conductance

# Skin Effect

- High Frequency Current Flows Primarily on the Surface of A Conductor
- Changing Current Distribution Causes Resistance to Increase As Function of Frequency



$$\delta = \sqrt{\frac{\rho}{\pi F \mu}}$$

Frequency

Resistivity

Permeability of Free Space

# Dielectric Absorption

- High Frequency Signals Excite Molecules in the Insulator
  - Insulator Absorbs Some of the Signal's Kinetic Energy
  - Signal's Magnitude Is Attenuated
- Dielectric Absorption Often Specified in Terms of Loss Tangent,  $\tan(\delta)$
- Lower  $\tan(\delta)$  = Less Losses

Material	$\epsilon_r$ at 1MHz	$\epsilon_r$ at 1GHz	$\tan(\delta)$ at 1 GHz	Relative Cost
FR4	4.30	4.05	0.020	1.0
GETEK	4.15	4.00	0.015	1.1
Rogers 4350/4320	3.75	3.6	0.009	2.1
ARLON CLTE	3.15	3.05	0.004	6.8

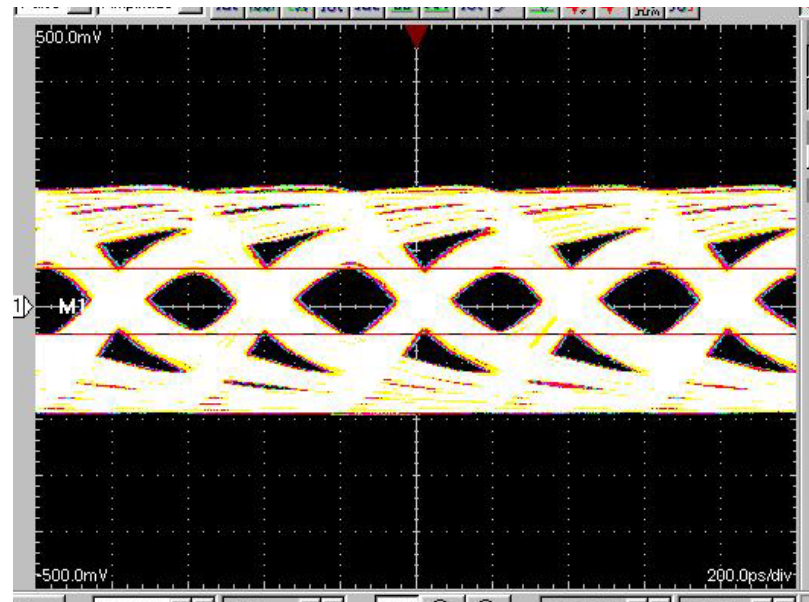
# Inter-Symbol Interference (ISI)

- Residual Voltages on Transmission Line that Can Interfere with Signals Traveling At Later Time
  - Reflections Off Impedance Discontinuities in the Transmission Line
  - Resonant Transmitter (LC Tank Circuit)
  - Inertial Delay & Hidden State (RC Circuit)
- ISI Degrades Signal Integrity of Transmission Line
  - Closes the Eye



# Example Eye Diagrams

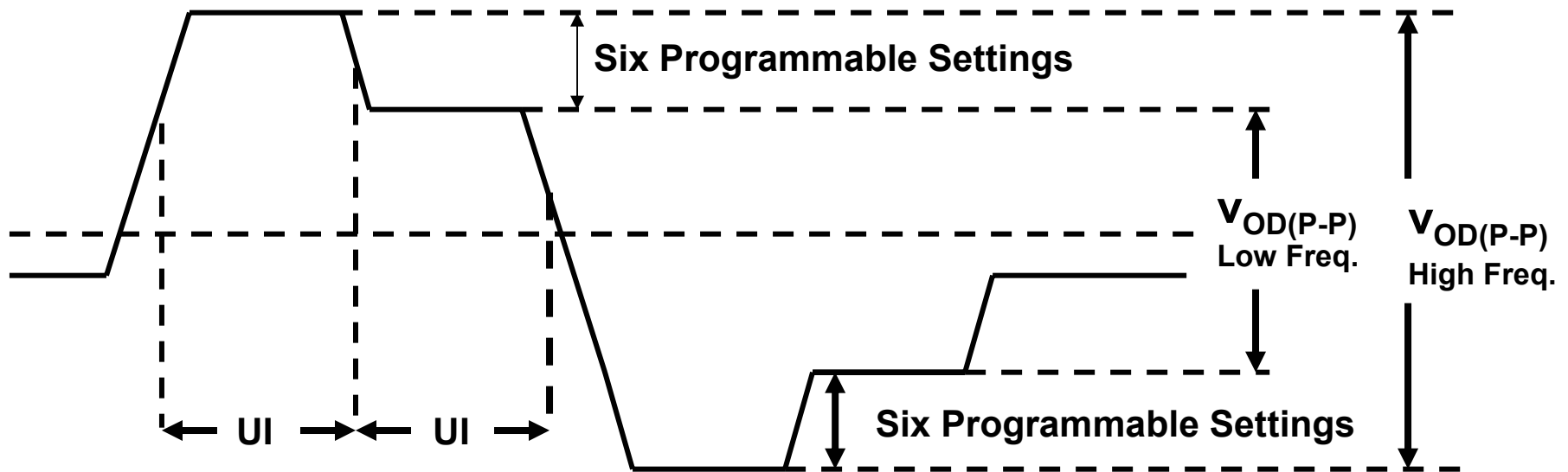
Eye Diagrams after 2", 22" & 36" of Backplane



Eye after 36" of FR4

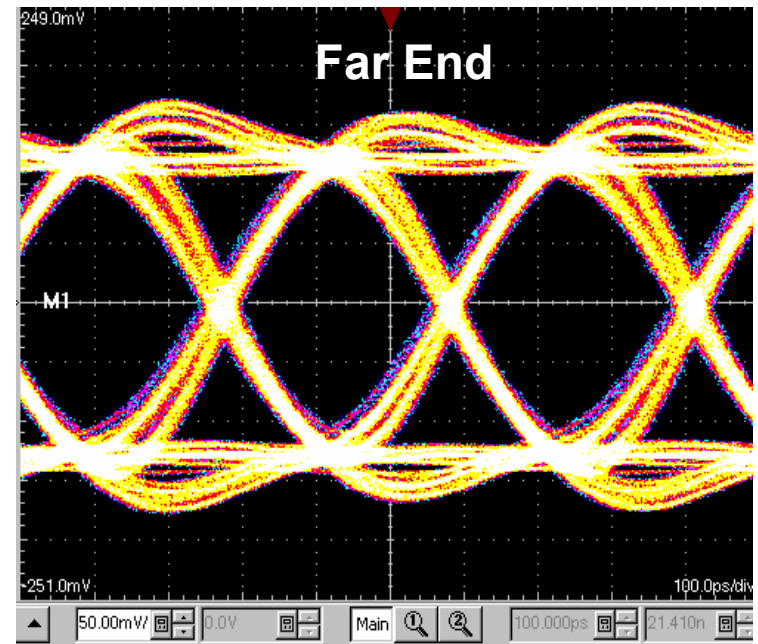
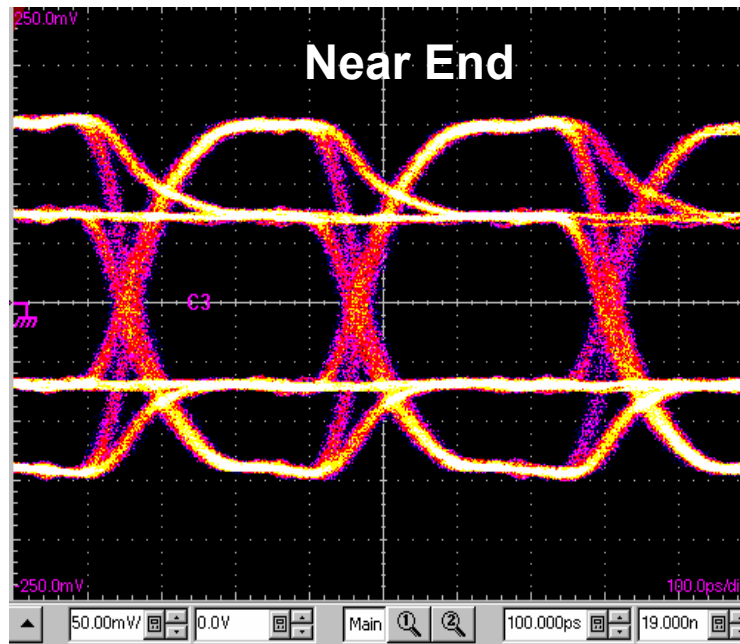
# What Can We Do About it?

- Programmable Pre-Emphasis!
- Boost High-Frequency Components to Reduce PDJ
  - When Switching Occurs the Differential Drive Is Increased
  - 6 Settings from 0% to 140% Based on  $v_{OD}$  Setting



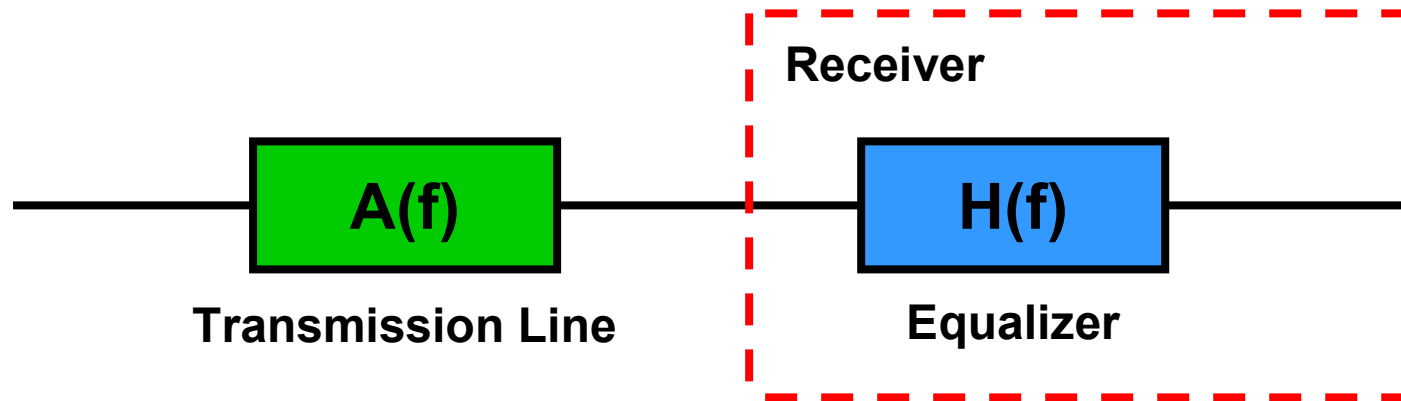
# Pre-Emphasis Opens the Eye

- 40" Backplane
- $V_{OD}$  of 400 mV
- Pre-Emphasis Setting = 4

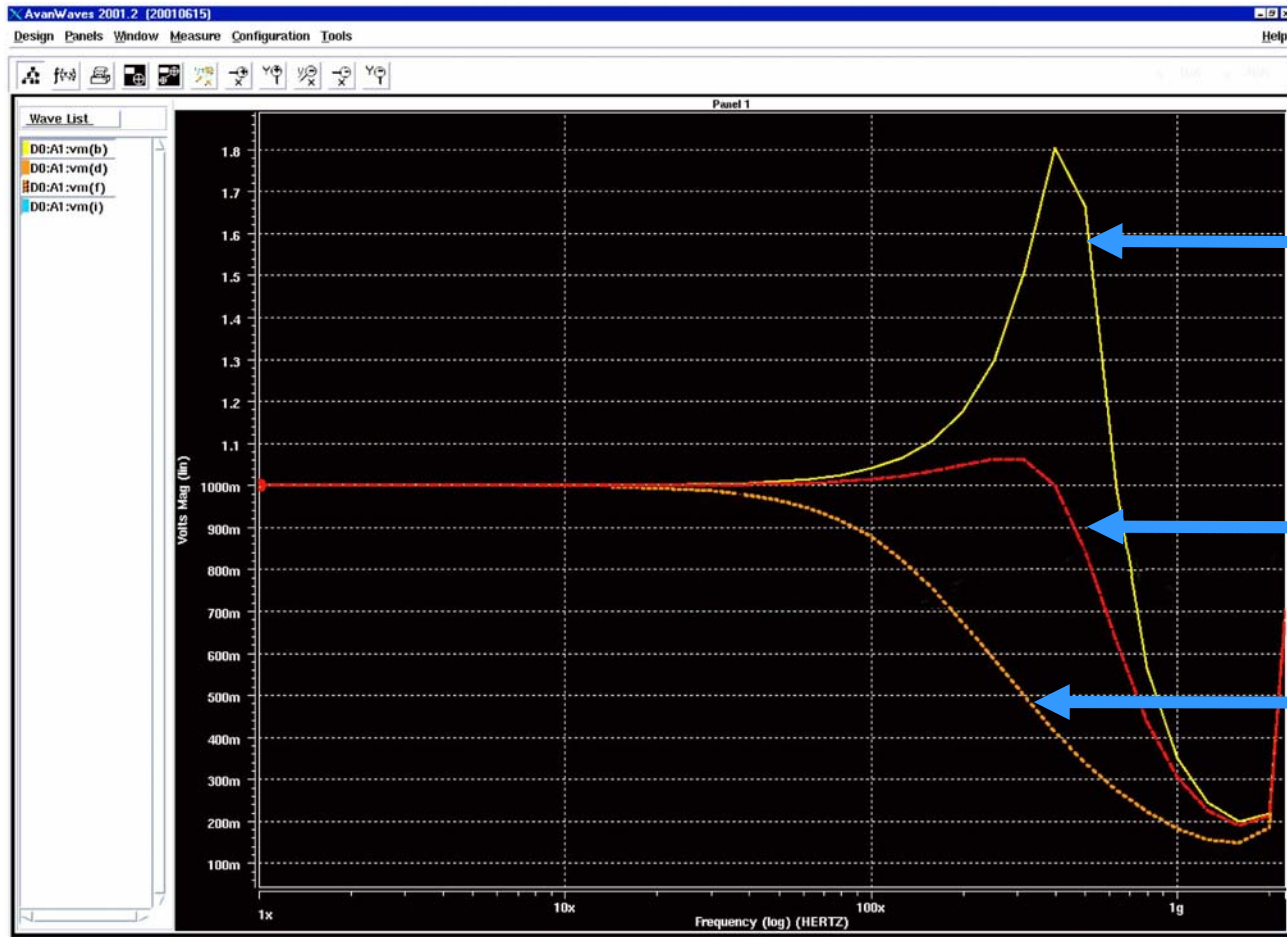


# Programmable Equalization

- Programmable Equalization Boosts Gain of Higher Frequencies At Receiver to Negate Effect of High-Frequency Losses
- Stratix GX Equalizer Can Be Programmed for Either 0", 10", 20", 30" or 40" of FR4 Trace
- Programmable Equalizer Can Boost Signals by Up to 9db



# Equalizer Frequency Response



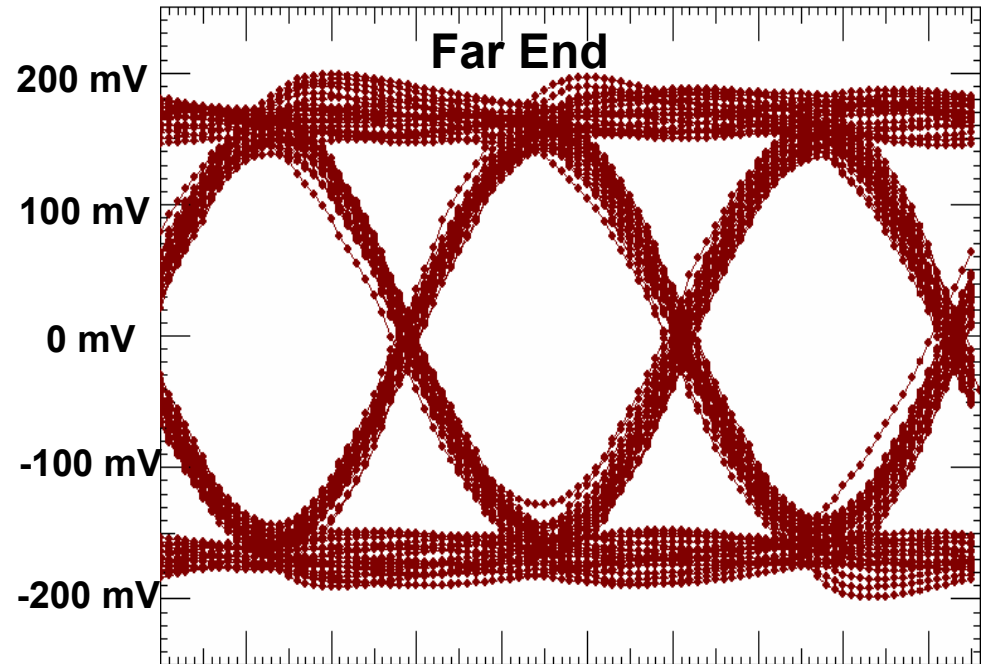
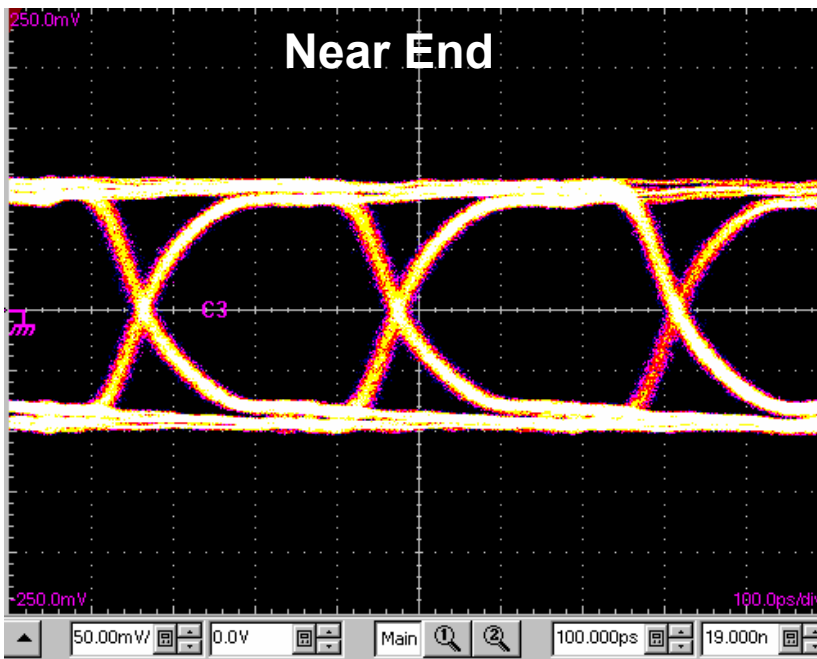
Equalizer

Equalizer+  
T-Line

T-Line

# Equalizer Opens the Eye

- 40" Backplane
- $V_{OD}$  of 400 mV
- Equalizer Setting = 40"

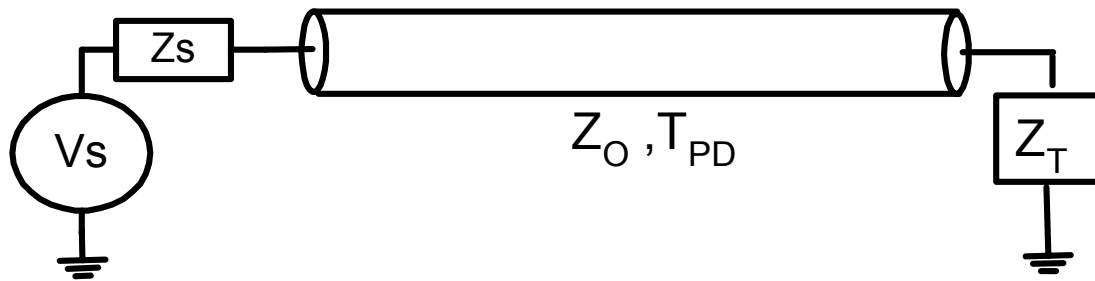


# Effects of Improper Termination

- The Ratio of Reflected Voltage Amplitude to the Incident Voltage Amplitude Defined As Reflection Coefficient, ( $K_r$ ):

$$k_r = \frac{V_R}{V_I} = \frac{Z_T - Z_O}{Z_T + Z_O}$$

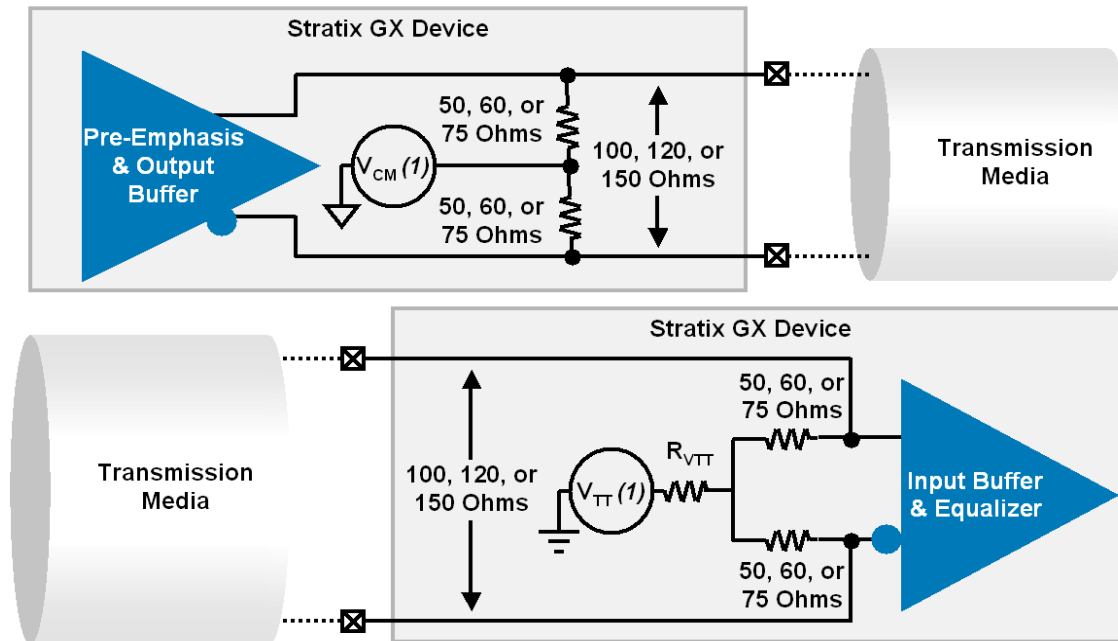
- In General,  $K_r$  Is Determined by Telegrapher's Equation





# Programmable On-Chip Termination

- Stratix GX Devices Offer Differential Programmable Termination of 100, 120, 150 Ohms for Both Receivers & Transmitters
- Termination for Channels Can Be Chosen Independently
- Tx & Rx Termination on Same Channel Chosen Independently





# Programmable Drive Strength

*Programmable VOD(p-p) Settings from 400 to 1,600 mV*

Programmed Output Current (mA)	V <sub>OD(p-p)</sub> at 100 Ω	V <sub>OD(p-p)</sub> at 120 Ω	V <sub>OD(p-p)</sub> at 150 Ω
4	400	480	600
8	800	960	1,200
10	1,000	1,200	1,500
12	1,200	1,440	-
14	1,400	-	-
16	1,600	-	-



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# Board Design Issues

# Board Design

- Not Your Average Low-Speed Board
- Very Observable Cause & Effects
- High-Speed Line Routing
- Return Paths
- Decoupling of Power Supply Noise
- Layer Stackup & Spacing

# Board Layer Stackup

Layer Number	Layer Type
1	Top Signal (50 Ohm)
2	GND
3	Signal (50 Ohm)
4	Signal (50 Ohm)
5	Power
6	Signal (50 Ohm)
7	Signal (50 Ohm)
8	PLL GND
9	Signal (50 Ohm)
10	Signal (50 Ohm)
11	Power
12	Signal (50 Ohm)
13	High-Speed Signal (100 Ohm)
14	High-Speed GND
15	High-Speed Signal (100 Ohm)
16	Signal (50 ohm)
17	Power
18	Bottom Signal (50 ohm)

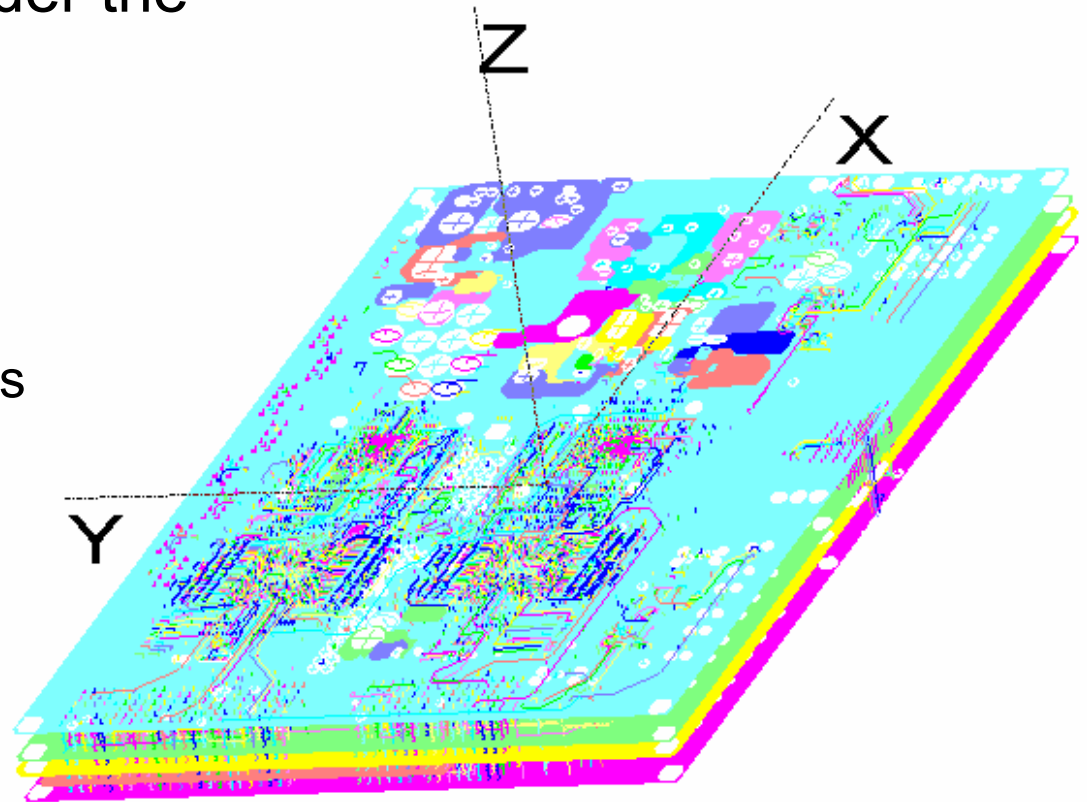
# High-Speed Transmission Lines

- Seamless Data Transfer: 50 Ohm Environment
- Remember Telegrapher's Equation?

$$k_r = \frac{V_R}{V_I} = \frac{Z_T - Z_0}{Z_T + Z_0}$$

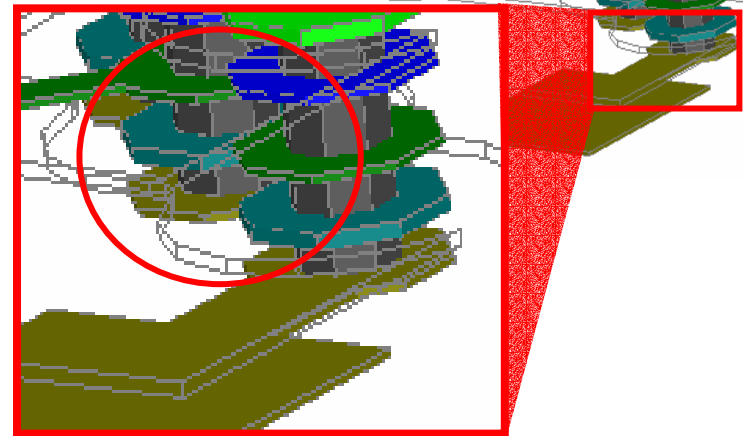
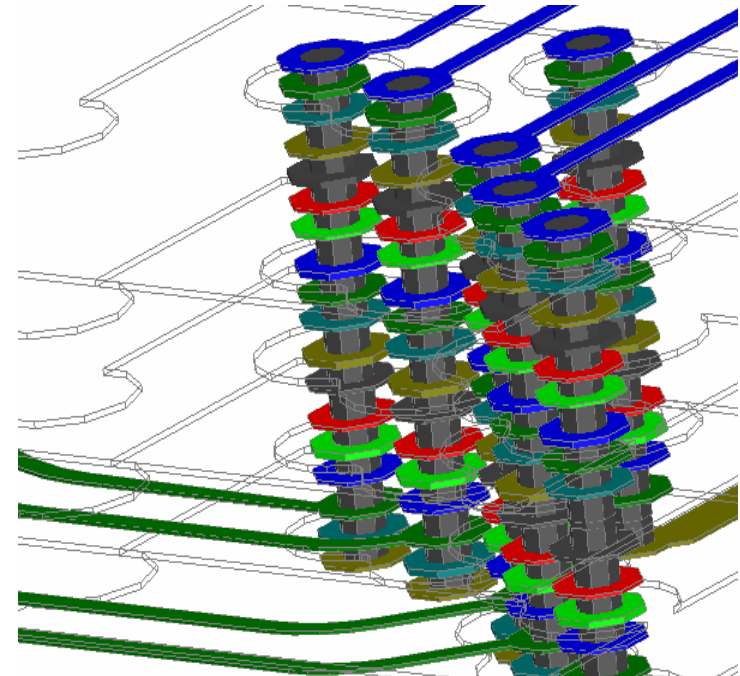
# Discontinuities

- When Dealing with Discontinuities on the Board, Consider the Following Factors
  - Right-Angle Bends
  - Vias
  - Connectors
  - Improper Terminations



# Vias

- Things to Worry about
  - Stub Is Created At the Via
  - Effect of Stubs: Inductance Is Small. Flux Lines Cancel At End of Via Due to the Whole Signal Reflecting
  - An Inductive Discontinuity Is Created on the Line Due to Improper Return Paths



Stub

# Vias

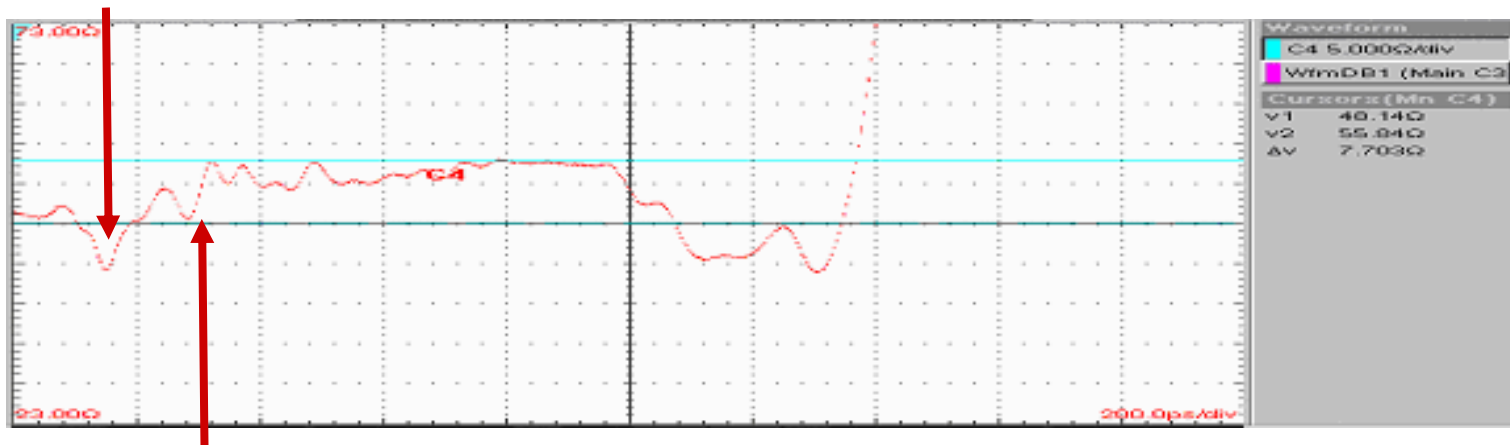
- Cannot Avoid Vias
  - Routing Issues
  - Impedance Control on Top Layer
- Use As Much of the Via As Possible to Reduce Stub
- Back Drill or Blind Vias to Eliminate Stub, But Expensive
- Ground Vias around Signal Via, Control Inductance
- For 3.125-Gbps Signal Board Thicknesses of 150 Mils & above, Vias Play Big Role



# Connectors

- Connectors on Transmission Paths Are Discontinuities
  - Based on Type of Connector They Can Be Either Capacitive or Inductive Discontinuity

## Capacitive Dip Due to Connector

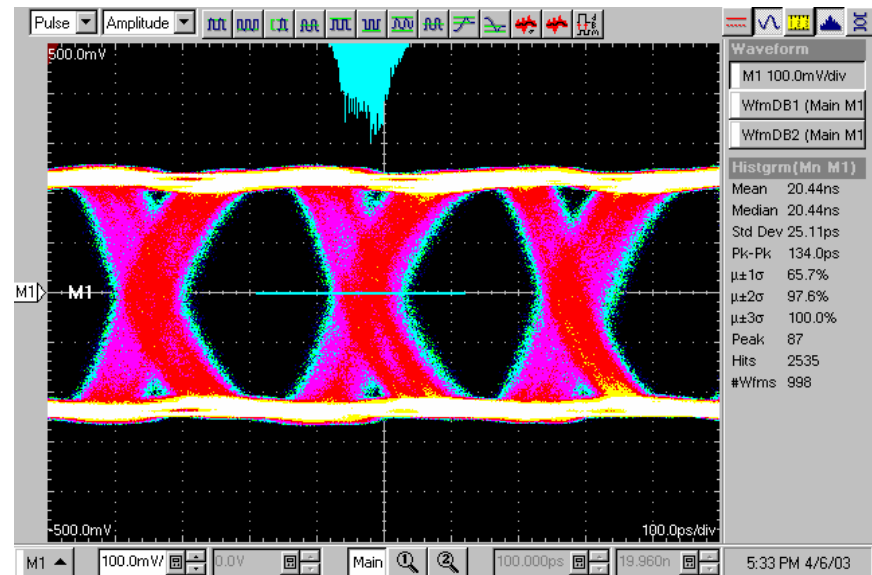


## Capacitive Dip Due to Via

# Decoupling

- Resonant Tanks Due to Parasitic Impedances
- Spikes Caused by Data Edges Induce Oscillations in Power Supply Voltages
  - Oscillations Over a Range of Frequencies
- Noisy Power Supply => Increased Jitter

## *Stratix GX Eye with Poor Decoupling*



# Decoupling

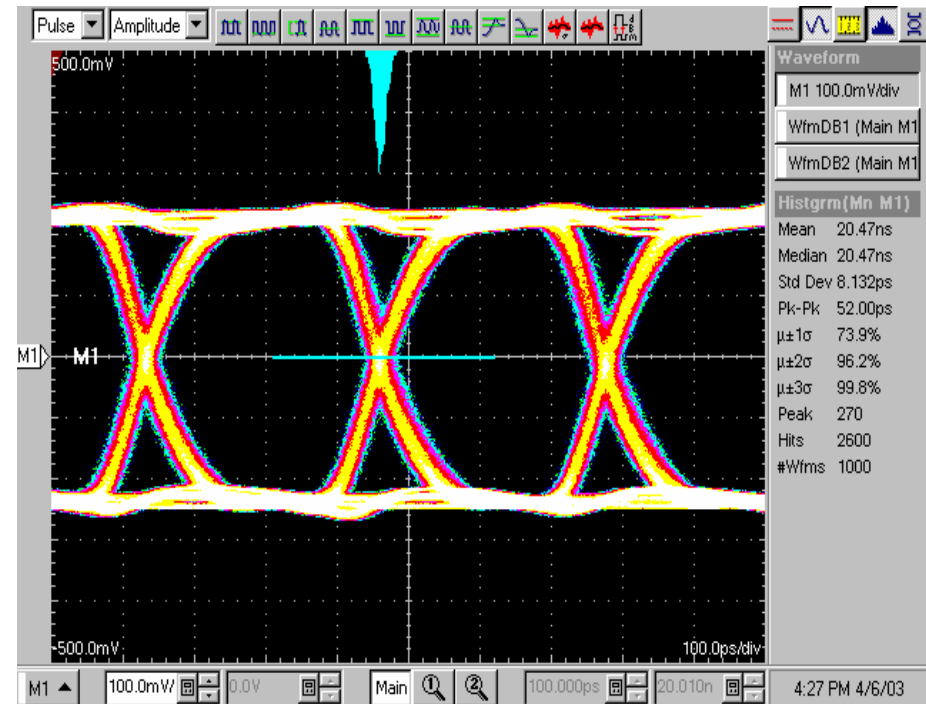
- Need to Filter Out the Noise Using Bypass Capacitors
  - Use a Range of Capacitance Values to Cover Frequency Range ( Example: 0.01  $\mu\text{F}$  to 200  $\mu\text{F}$ )
- Increasing Influence of Parasitic Inductance with Frequency
- Need for Power-Ground Plane Capacitance
  - Capacitance Due to Parallel Plate Capacitance
  - Minimal Parasitic Resistance & Inductance

$$\text{Parallel Plate Capacitance} = \epsilon_0 \epsilon_r (A/d)$$

# Decoupling Recommendations

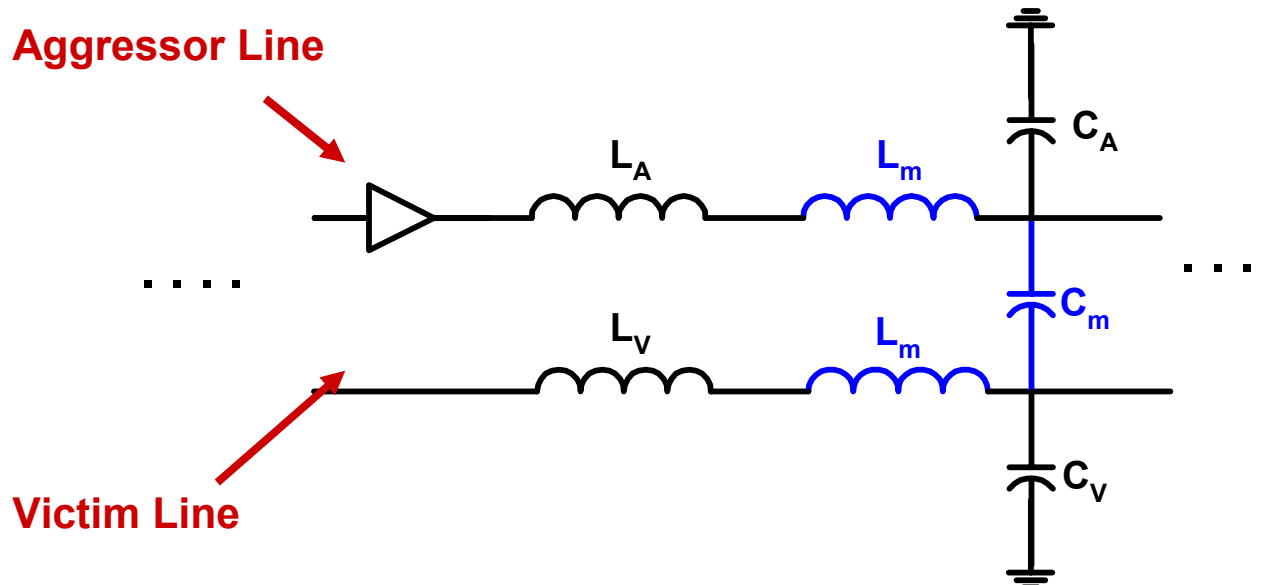
- Locate the High Frequency Decoupling Capacitors As Close to the IC As Possible
- Bulk Capacitors Can be Placed Farther Away
- Use Power – Ground Plane Capacitors As Much As Possible
- Use Low Inductance Capacitors

## *Stratix GX Eye with Effective Decoupling*



# Crosstalk

- Crosstalk Is Modeled by Super Positioning Mutual Inductance & Capacitance onto Existing Transmission Line Model



Segment of Lossless Transmission Line with Crosstalk Coupling Effects

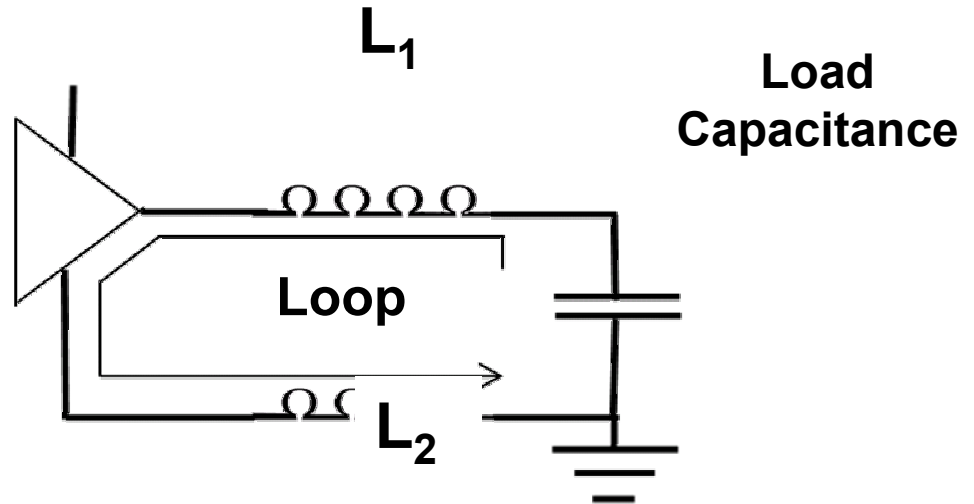
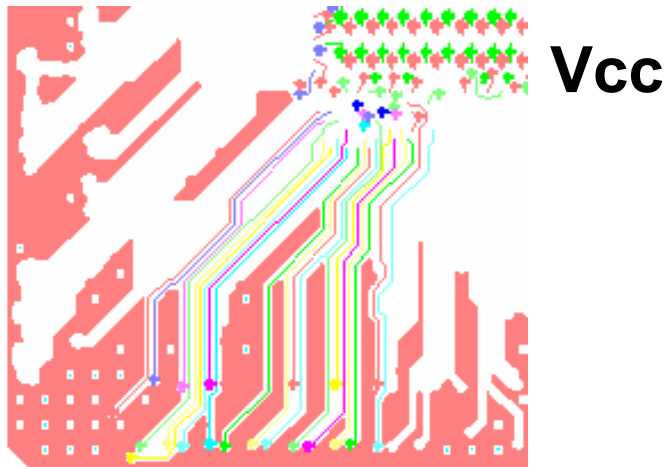
# Crosstalk & Termination

- How Can You Reduce Noise Caused By Crosstalk?
  - Crosstalk Is A Proportional Noise Source, So Increasing the Signal Swing Will Only Increase Amount of Coupling Noise
  - Both Near-End & Far-End of Line Needs to Be Terminated to Reduce Noise Caused By Crosstalk
  - Lines Spaced Sufficiently Apart; EM Simulations



# SSO Noise

- Drivers Switch High to Low
  - Ground Bounce Occurs
  - Also Power Collapse Occurs
- Higher the Inductance, Higher the G B Voltage ( $V = L (di/dt)$ )
- Higher the Inductance, More the Power Collapses
- More I/O Switching Requires More Regional Energy

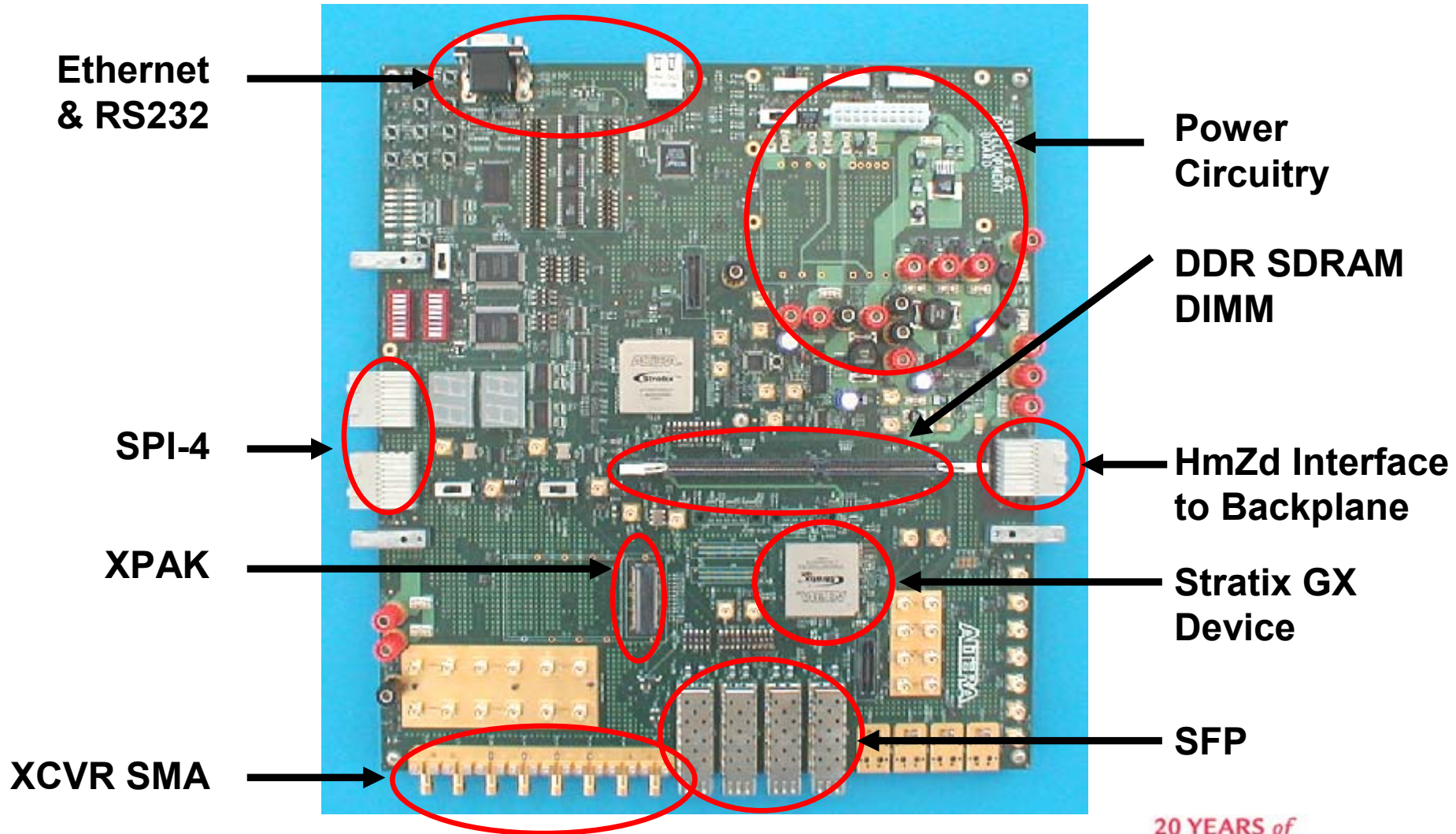


# How to Reduce SSO Noise?

- Spread Out I/O Pins Being Used
  - Use Different Power Pins
- Use Differential Signaling → Rejects Common Mode Noise
- Slow Down the Slew Rate of Driver ( $di/dt$ )
  - This Reduces  $V = L (di/dt)$
- Use Programmable Grounds/ Supply
  - Tie Unused I/O Pins to Ground / VDD

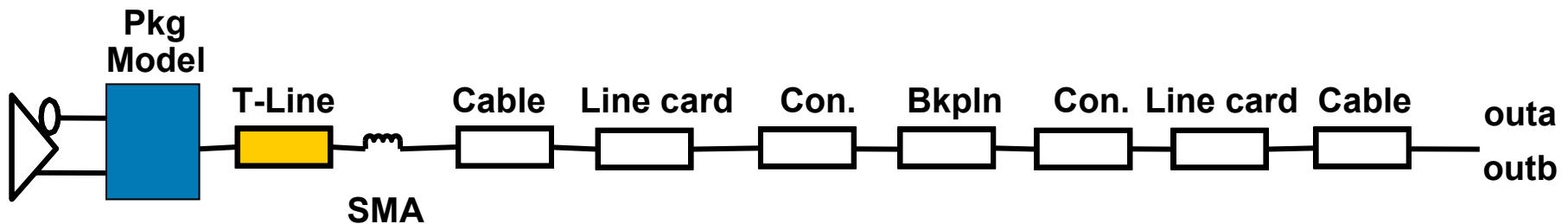


# Stratix GX Applications Board



# Signal Integrity Simulation Tools

- Chip-Level Simulations → HSPICE
- HSPICE Still the Most Reliable High-Speed Simulator
- Need to Accurately Model the Transmission Medium
  - Transmission Lines, Vias, Connectors
  - RLGC Parameters Imported to HSPICE

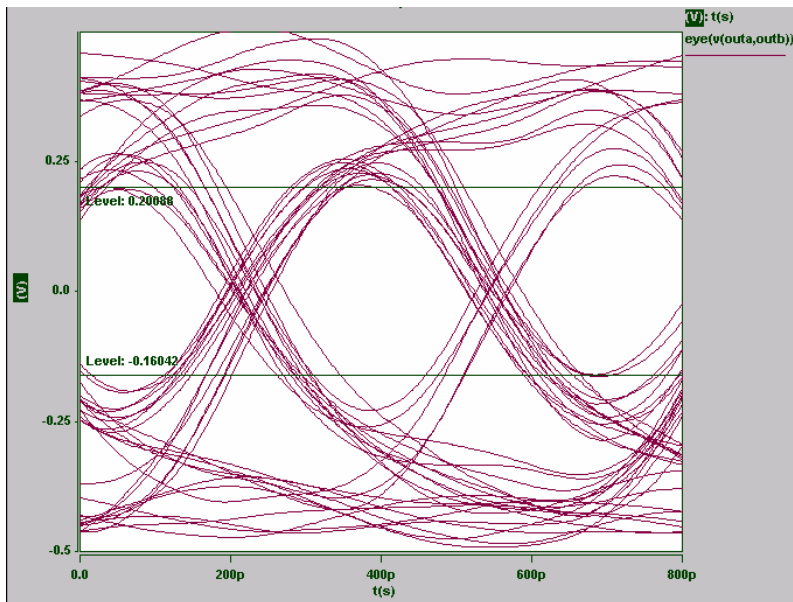


# Signal Integrity Simulations

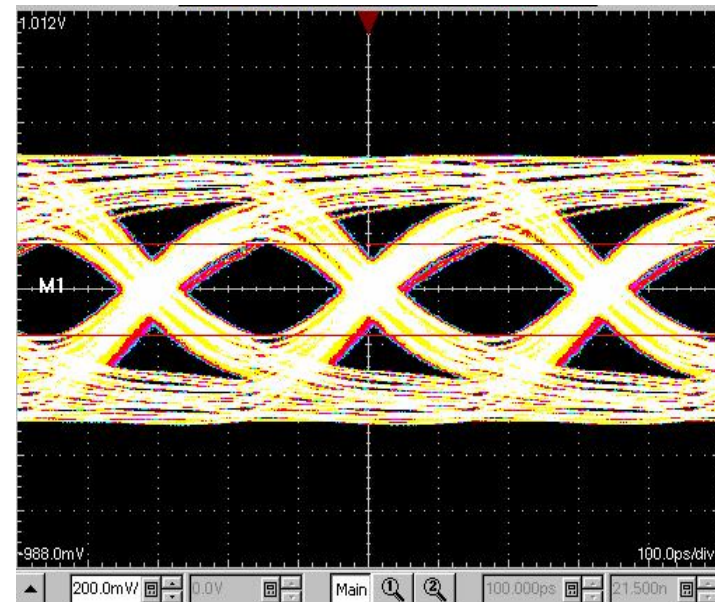
- EM Field Solvers Used to Extract Board Models
- Assign Conductor & Dielectric Materials
- Setup Solution Parameters
  - Inductance, Capacitance, Impedance & Admittance
- Solve Parameters
- Check Solution for Various Parameters
  - Characteristic Impedance, RLGC Values, Propagation Delay, Crosstalk, Skin Effect

# Simulation Vs. Measurement

**Conditions: Stratix GX Device Driving 20" of XAUI Backplane (Connectors & Daughter Card Included)**



**Simulation**



**Measurement**

# Altera's Support Structure

- Altera Provides Simulation Models
  - HSPICE, VHDL AMS, DML (Soon)
- Board Layout Guidelines with Sample Layout
- Characterization Reports
- Complete User Guide
- High-Speed Expert Customer Support

# Summary

- Serial Communication Is the New Standard
- Many Protocols Available to Implement System
- Pre-Emphasis & Equalization Make Huge Impact
- Careful Design of Board for High-Speed Signaling Is Critical
- Many Tools Available to Ensure Successful Design Implementation



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