ALDEC
The Design Verification Company

Accelerated Hardware/Software Co-Verification Solution for NIOS Active-HDL w/ CoVer

SOPC World 2004

Corporate Background

- Established in 1984
- Mixed VHDL, Verilog, SystemC, SystemVerilog and EDIF verification in a single simulation kernel
- Graphical Design Entry and Debugging Tools for HDL designers
- Hardware-based acceleration for SOC designs

Aldec products include:

- **Active-HDL**
- **Riviera**
- **Riviera-IPT**
- **CoVer**

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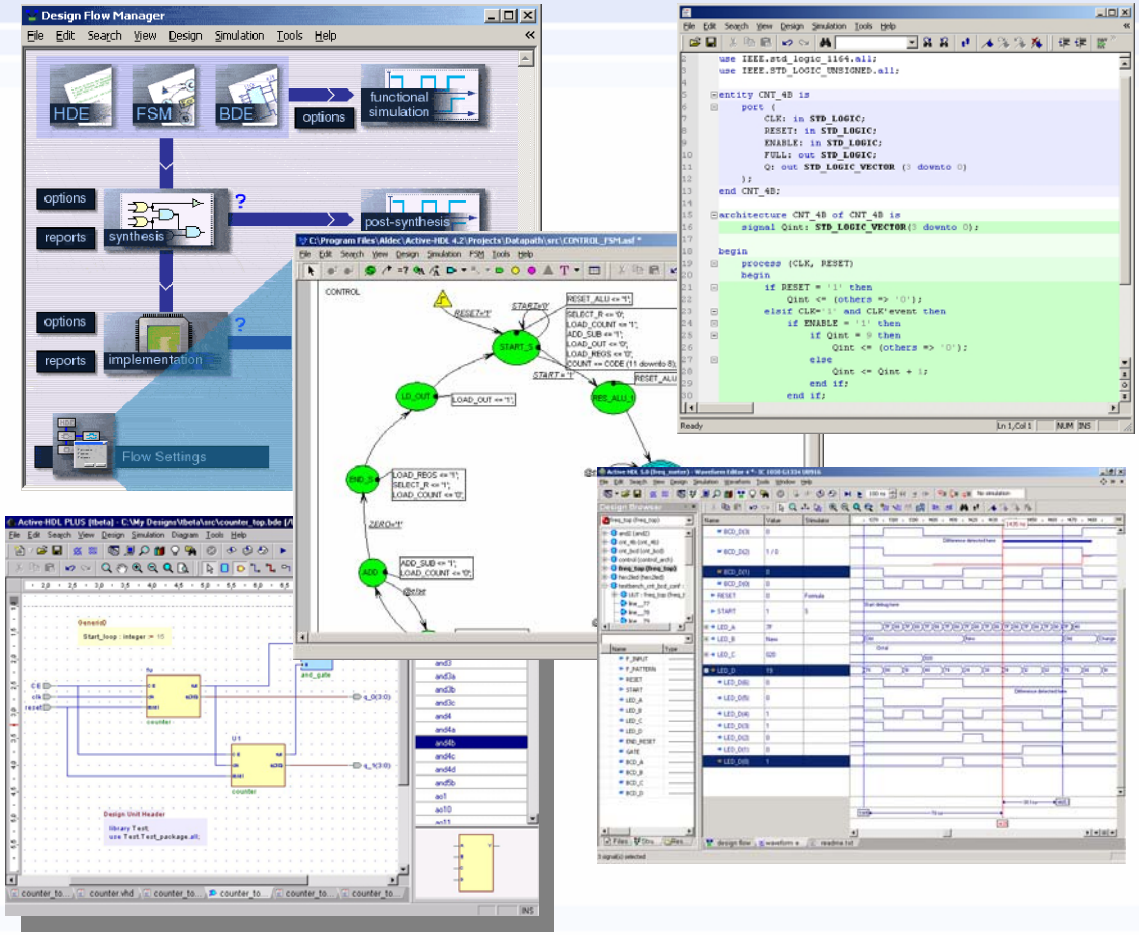
Active-HDL Design Desktop

- **Design Entry**
  - Block Diagram Editor
  - State Machine Editor
  - HDL Editor
  - Design Flow Manager
- **Design Verification**
  - VHDL/Verilog/SystemC and EDIF Simulator
  - Graphical Source Debugger
  - Testbench Generation
  - Waveform Editor
  - Timing Simulation



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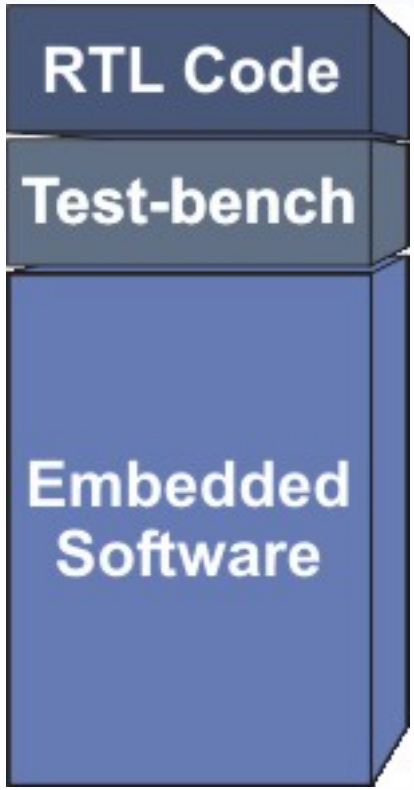
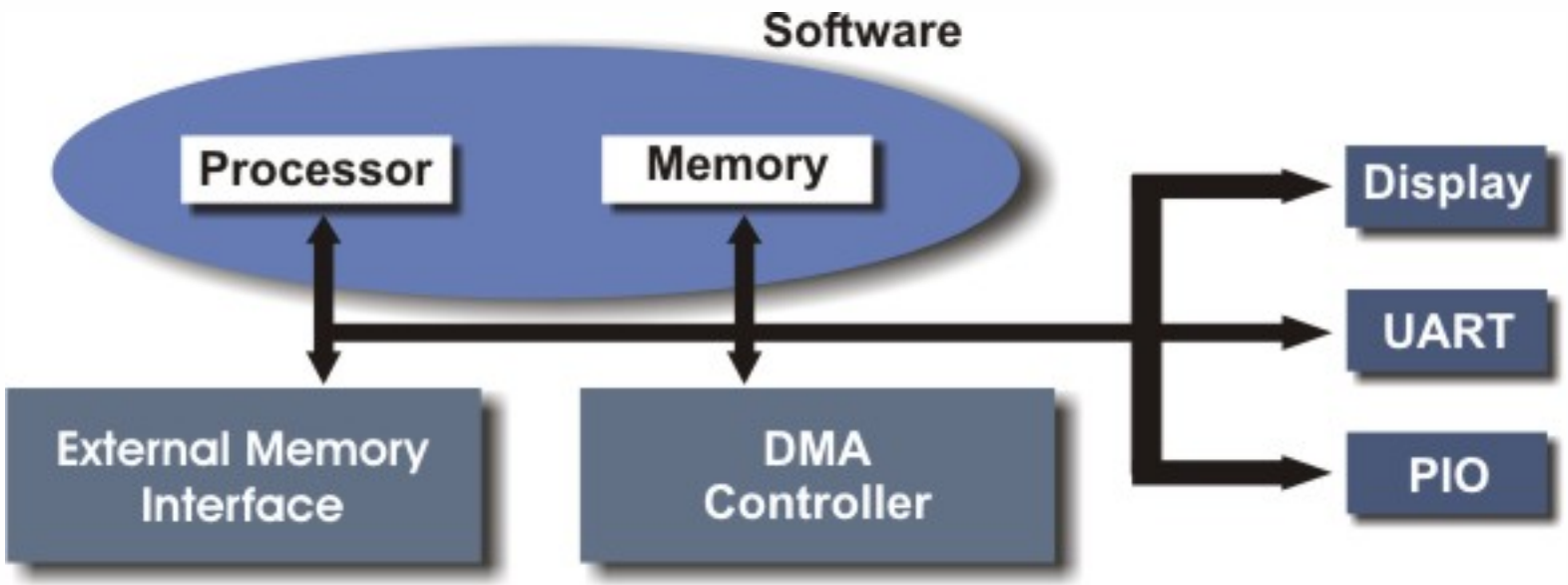
Todays SOC Verification Challenges

Hardware System Development



Embedded System Development

Embedded System Architecture



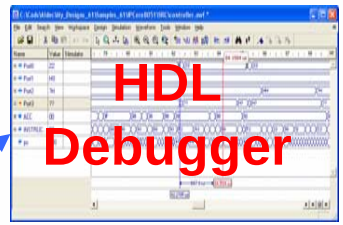
The software content is increasing. A system-on-a-chip designed today typically runs an operating system and some user applications

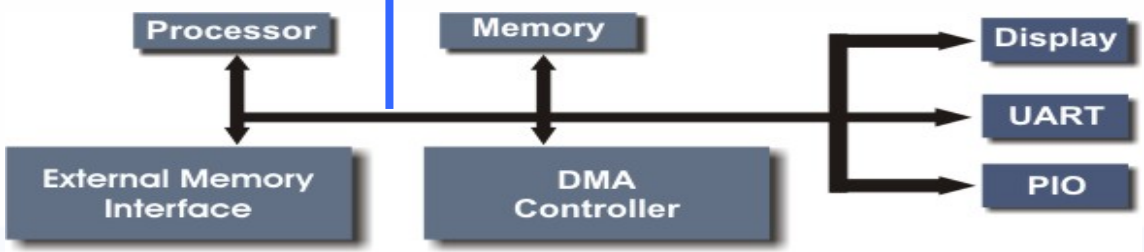
SOC Verification in HDL Simulator

- Hardware Team requires:
  - Accuracy at the bus level ✓
  - HDL debugging environment ✓
  - Performance ✗
- Software Team requires:
  - Software debugging environment ✗
  - High performance to execute large chunks of code ✗

Typical HDL Simulation Environment

SOFTWARE DEBUGGER *not available*

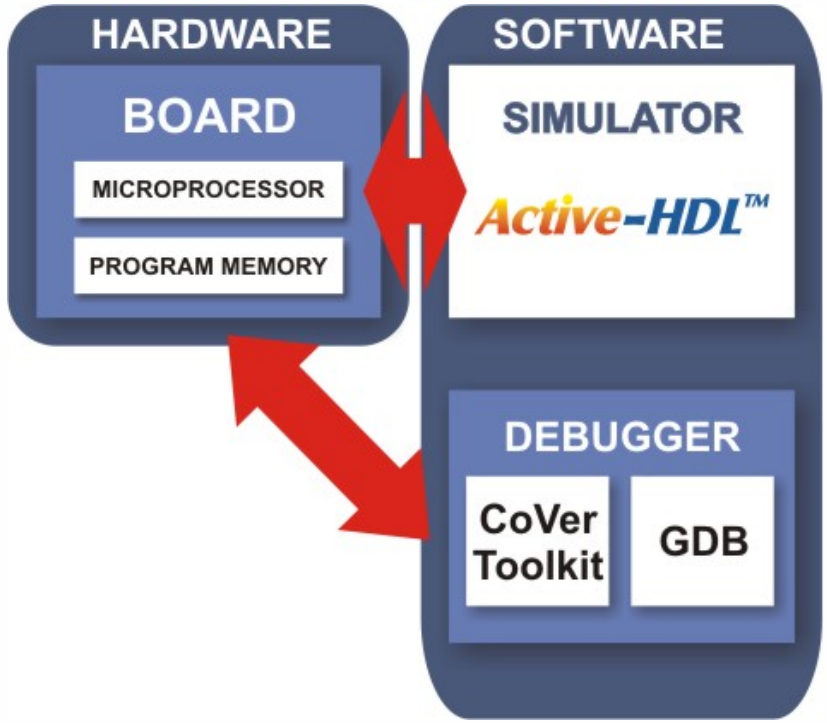




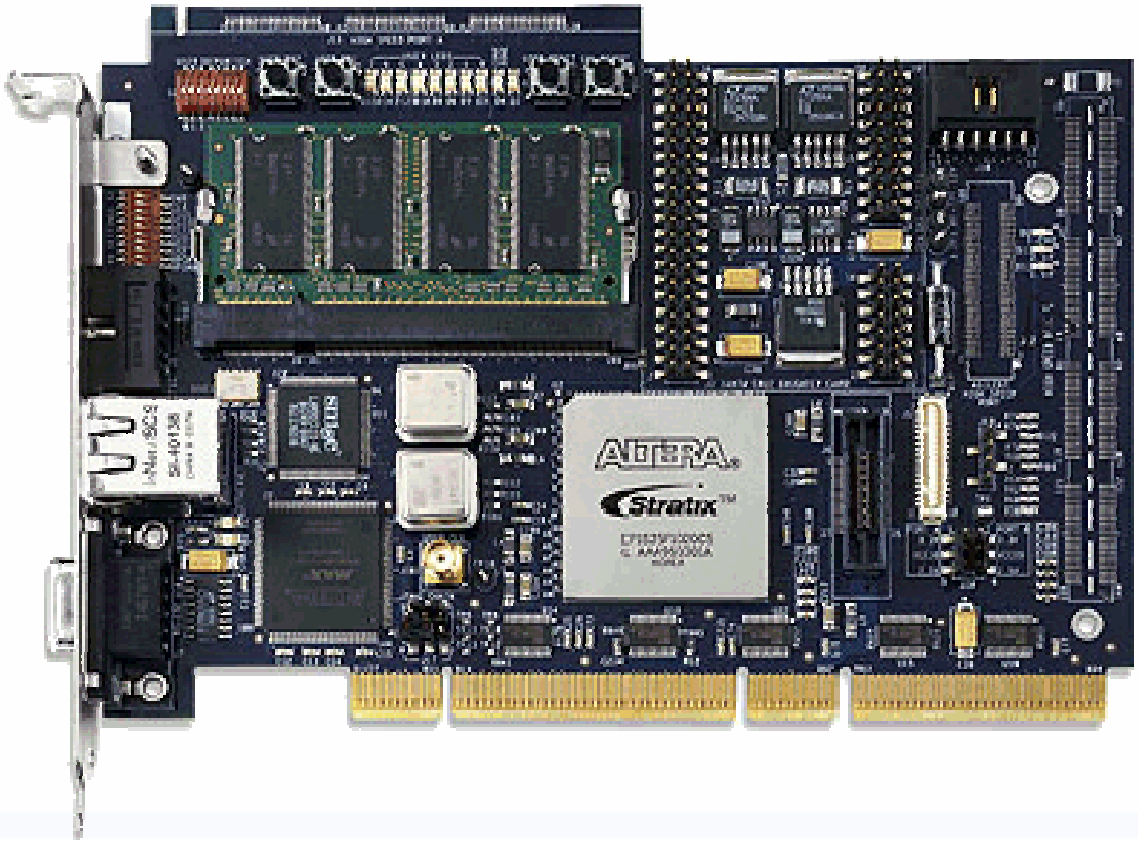
100 instr./s

Active-HDL w/ CoVer Environment

- **CoVer is installed in conjunction with Active-HDL and Altera's embedded system development kit (e.g. *SOPC Builder*)**
- **Install hardware board: PCI development board**
- **Installed software: drivers, interfaces and applets enabling communication with the board**



Altera™ PCI Development Kit, Stratix Edition (PCI-Board/S25) – Used for Co-Verification



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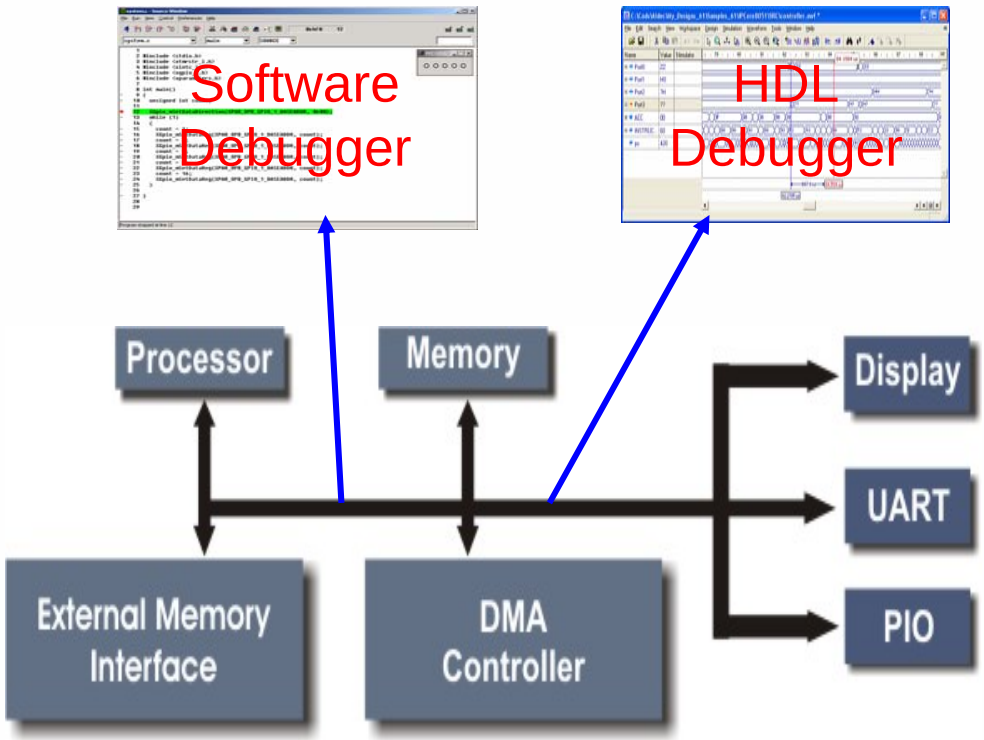
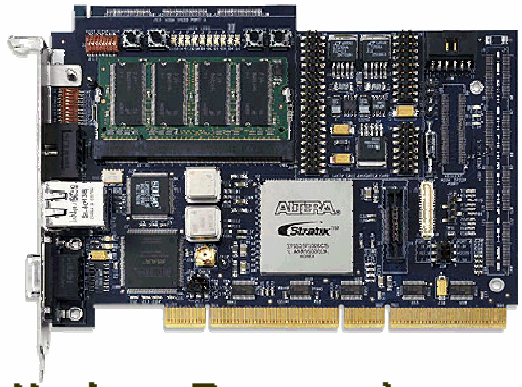
Benefits – Hardware and Software Teams

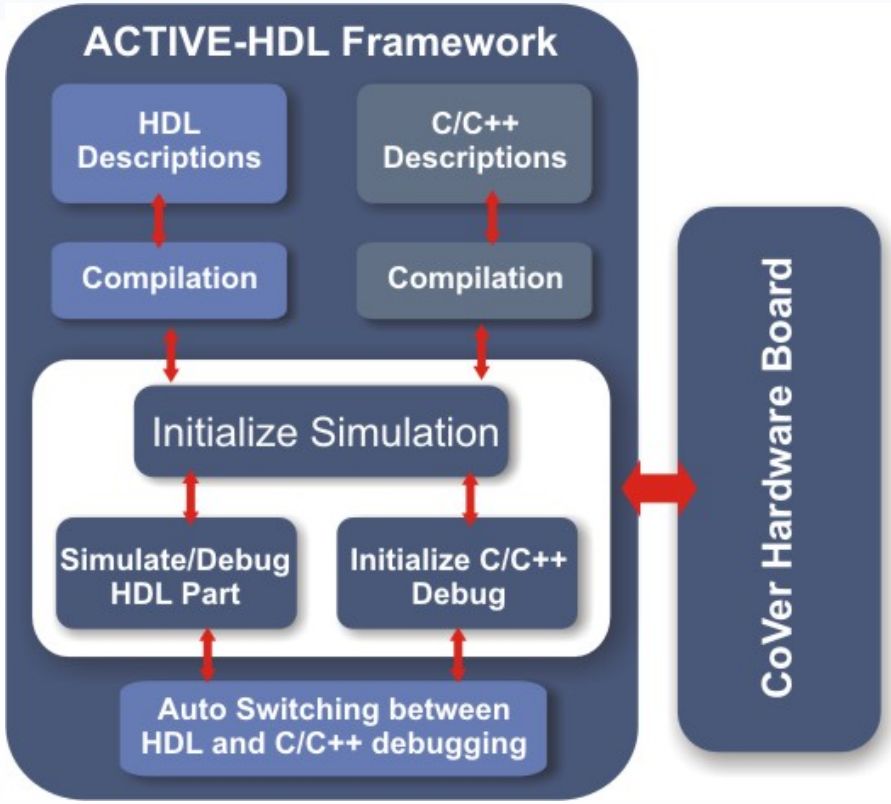




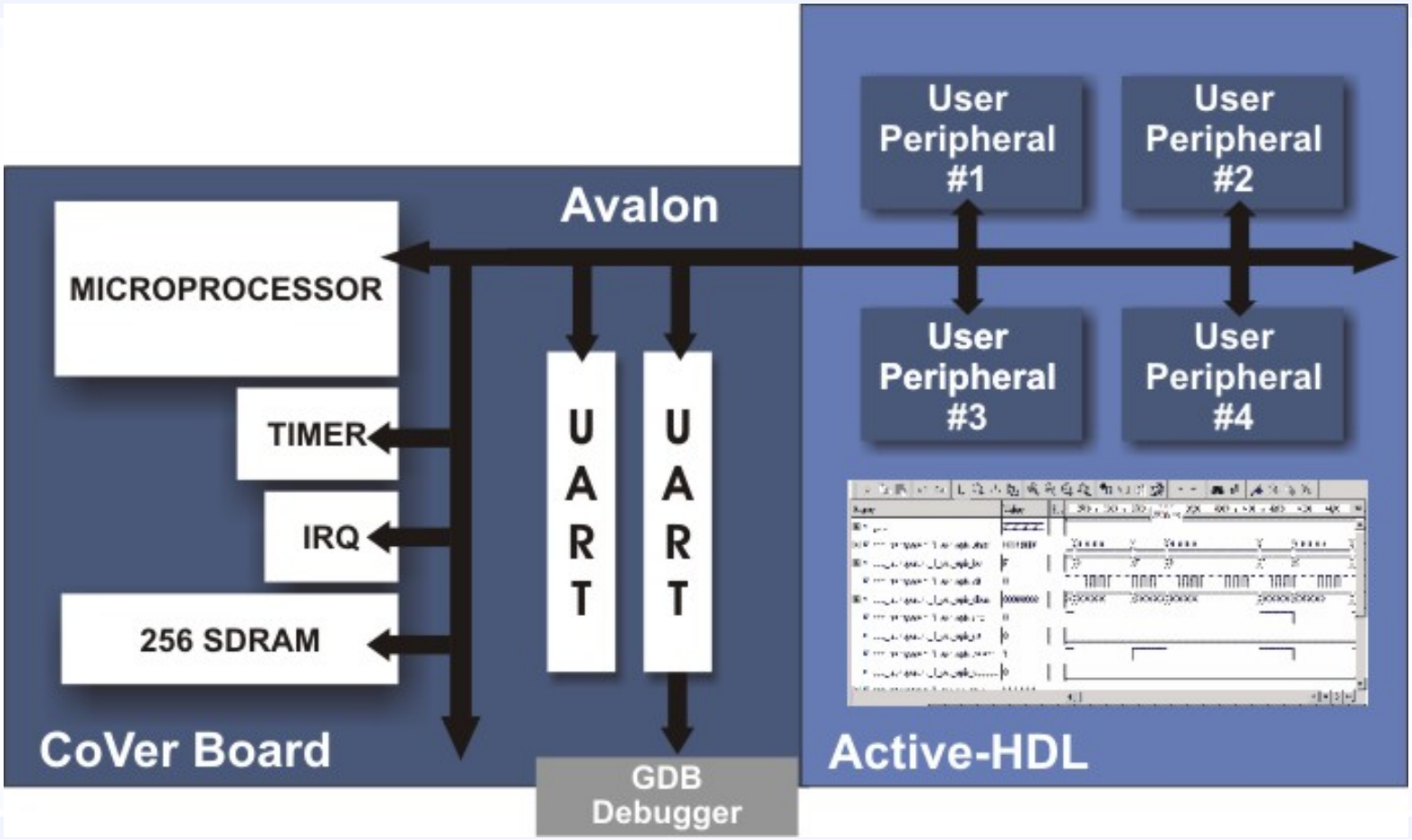
- **Hardware Team requires:**
  - **Accuracy at the bus level**
  - **HDL debugging environment**
  - **Performance**
- **Software Team requires:**
  - **Software debugging environment**
  - **High performance to execute large chunks of code**

Active-HDL w/ CoVer Design Flow

- **Both HDL descriptions of system peripherals and C code can be entered and compiled within Active-HDL framework**
- **Initialization of simulation pushes MPU and some other elements into the Altera device on the hardware board**



Verification Environment



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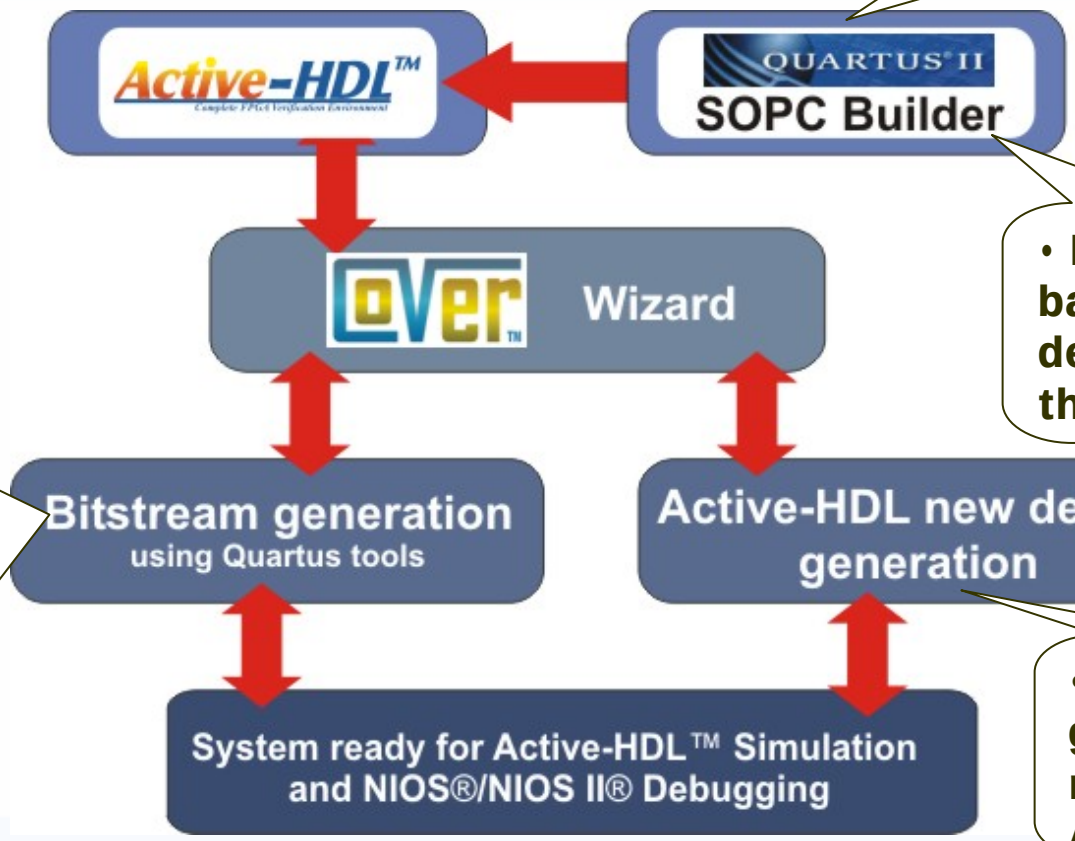
User Flow

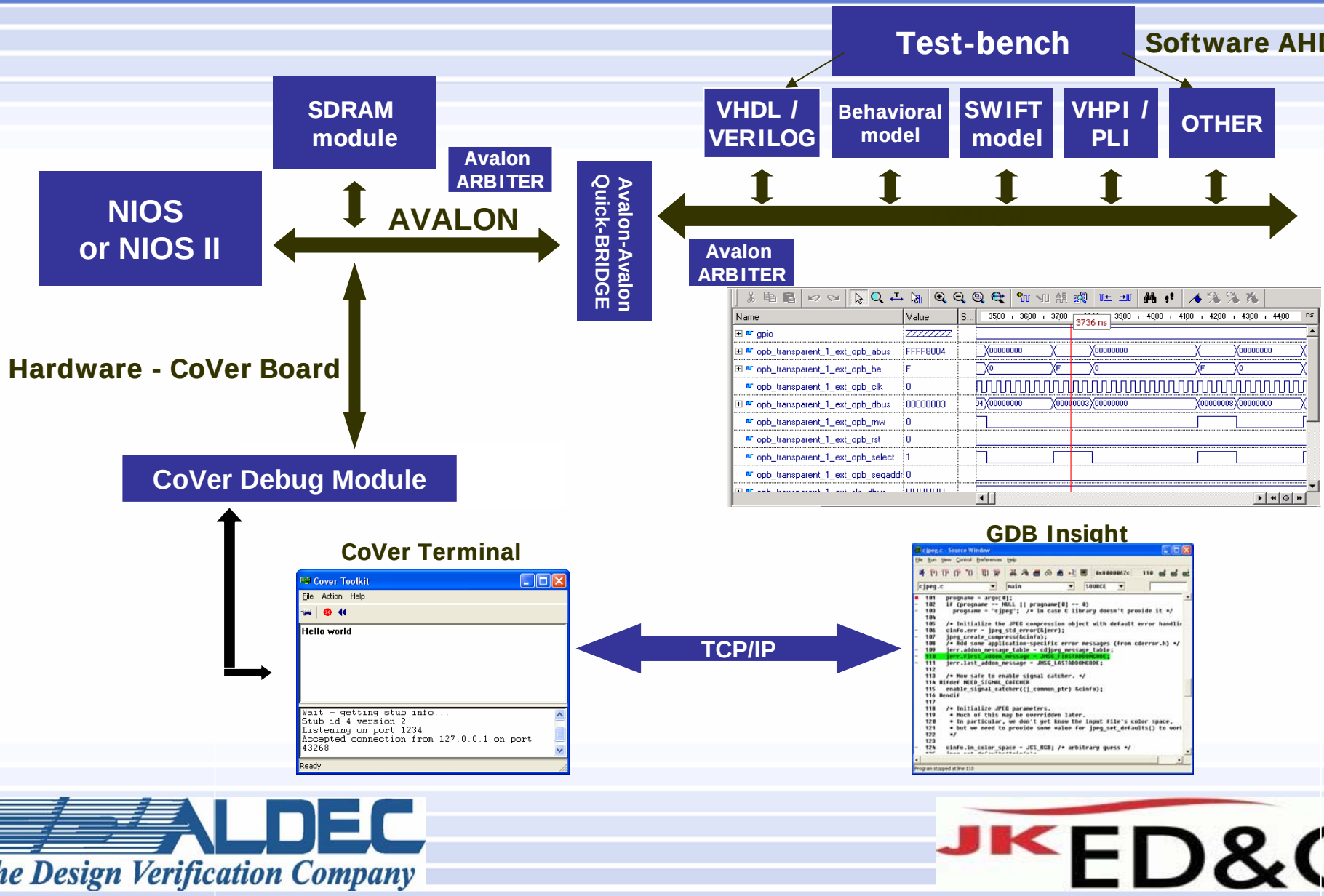


- CoVer wizard loads the PTF file and generates CoVer specific modules.
- Using Quartus proper bitstream is generated for CoVer board.

- Nios/NiosII based design developed by the SOPC user

- CoVer wizard generates ready to use AHDL design

System Diagram



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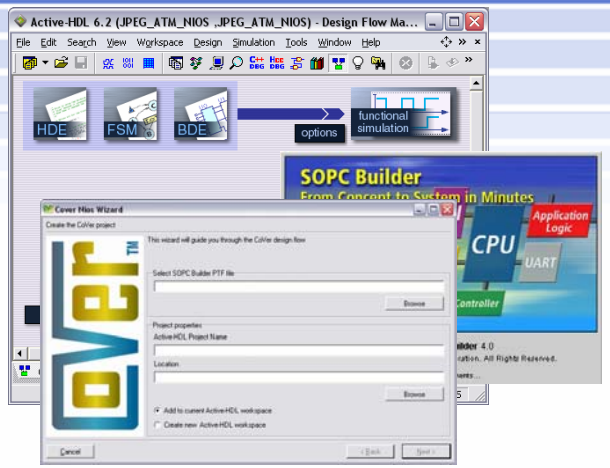
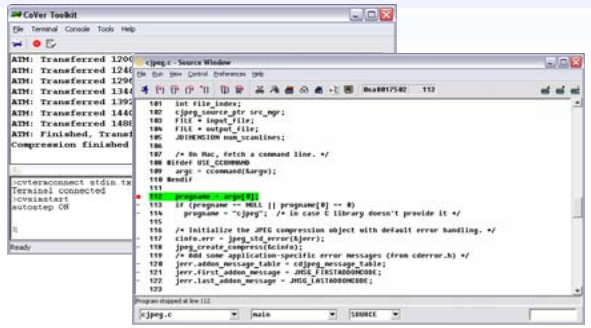
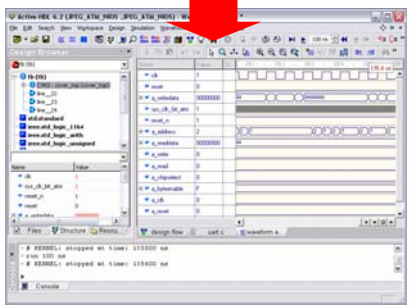
Co-Verification Environment

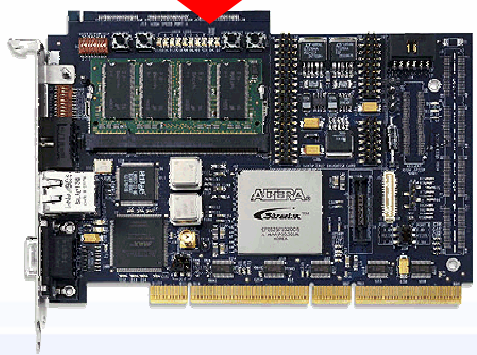




CoVer Nios/Nios II Wizard for Active- HDL™

Software Debugging for Nios™ or Nios II ™





Hardware Debugging for Active-HDL™

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Technical Parameters

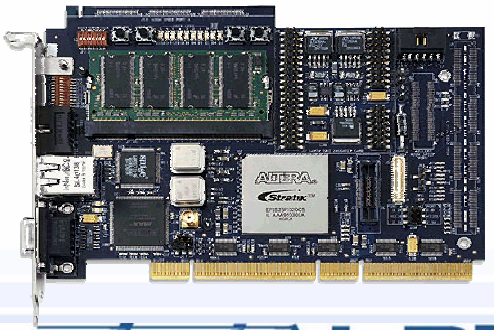
MicroProcessor	Nios or Nios II Core implemented in Altera Stratix (EP1S25)
Supported boards	Altera PCI Development Kit, Stratix Edition Aldec HES3-AS25EX
Memory	SDRAM, 256 MB
Hardware Clock	33 MHz
User Bus	Avalon BUS
Altera tools	Quartus II 4.1 and Nios 3.1 and higher
Nios debugger	GNU GDB Insight
Nios compiler	Nios-gcc
HDL simulator	AHDL6.3 and higher
Operation system	Windows 2k/XP

Sample Design Benchmark

HW

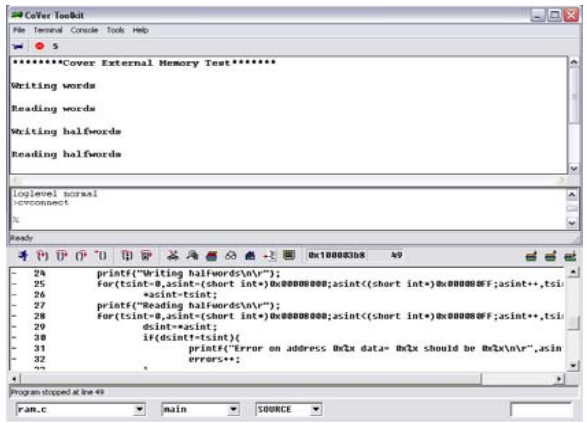
- Nios processor core
- Program and Data memories
- Debug UART
- STDIO UART

Time [s]



SW

Debug & IO modules



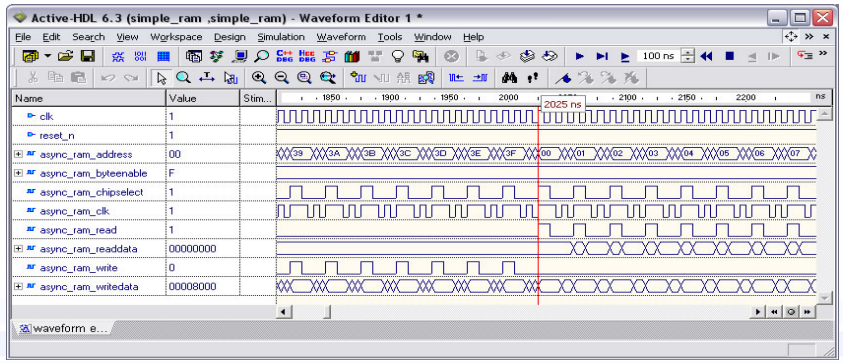
Simulation time:

Active-HDL: 246 seconds

Using CoVer: 3 seconds

Speed-up 82x

Simple_Ram core in software simulation



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Active-HDL w/ CoVer Benefits

- 100% visibility for debugging and verification
- Simulation is accelerated dramatically because a software simulator is not simulating the core
- There is no need for the hardware engineer to continually make prototypes for the software developer. This eliminates the time consuming runs of synthesis and implementation after each design iteration during the verification and design cycle
- Both the designer and the developer can work on the same configuration of the product in a common environment thus saving time and improving time to market
- When the processor is not communicating with the peripherals in software, high-speed performance is provided. Using patented Quick-Bridge technology the processor can run at emulation speed (MHz)