Implementing Video and Image Processing Designs Using FPGAs
Agenda

- Key trends in video and image processing
- Video and Image Processing Suite
- Model-based design for video processing
- Tutorial
Video and Imaging With FPGAs

- Broadcast Infrastructure
- HDTV Videoconferencing
- HDTV Display
- Medical Imaging
- Security DVR
- HD Security Camera
- Consumer/Auto Display
- Document Imaging
- Military Imaging
Key Trends in Video and Imaging

■ Higher resolutions
  – 3,000 x 3,000 (and higher): medical imaging, military, machine vision
  – 4,096 x 1,714: digital cinema
  – 1,920 x 1,080: HDTV, broadcast
  – 1,280 x 720: video surveillance, videoconferencing

■ Advanced video compression
  – H.264, JPEG2000, VC1
Current Solutions Do Not Deliver

- **Video/Imaging ASSPs**: Not optimized for target applications, Risk of obsolescence
- **DSP**: Cannot achieve high definition in single device
- **ASIC**: High development cost, Cannot keep up with fast-evolving applications
Altera’s FPGA Solution

- High performance in a single device
- Fast time-to-market
- Easy to upgrade
- Low development cost
- Obsolescence proof
- Lower unit costs at high volumes
Video Benchmarks

Cost Normalized to FPGA

1.00  2.00  3.00  4.00  5.00  6.00  7.00

- 7x7 2D Filter 720P
- 7x7 2D Median Filter 720P
- H.264 BP Encoder 720P
- H.264 BP Encoder 1,024x768
- 16-Channel H.264 BP Encoder CIF
- 4-Channel H.264 BP Encoder D1
- H.264 MP Encoder D1
- H.264 MP Encoder 1080i
- JPEG2000 Encoder D1

Colors:
- **FPGA**
- **HardCopy® II**
- **DSP Only**
# Altera Video and Image Processing Solutions Overview

## Video Reference Design

<table>
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<th>DSP Algorithm Design Flow</th>
<th>VHDL/Verilog</th>
<th>MATLAB/ Simulink DSP Builder Synplicity</th>
<th>‘C’ to Hardware Mentor Celoxica</th>
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<td>Altera and Third-Party Video I/O and Interface IP</td>
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<td>System Integration</td>
<td>SOPC Builder, VHDL/Verilog</td>
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<td>Devices and Dev. Kits</td>
<td>Cyclone® II, Stratix® II, HardCopy II</td>
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</table>
IP Examples – Video

**I/O and System**
- PCI Express
- Serial Rapid I/O
- EMIF Interface
- ASI
- SDI
- ATA HDD (Nuvation)
- MPEG2 Transport
- 10/100/1000 Ethernet
- DDR/DDR2 Controller

**Pre-/Post-Processing**
- Scaler
- Deinterlacer
- 2D FIR Filter
- 2D Median Filter
- Color Space Converter
- Chroma Resampler
- Gamma Corrector
- Alpha Blender
- Highest Quality HDTV Upconversion (Let It Wave)
- AES/DES/Sha-1 Encryption (CAST)

**Compression**
- H.264 MP, HP (ATEME)
- H.264 BP (4i2i, CAST, W&W)
- H.264 CABAC/CAVLC (ATEME)
- H.264 Loop Filter (ATEME)
- MPEG4 SP/ASP (CAST, Barco)
- JPEG (CAST, Barco)
- JPEG2000 (CAST, Barco, Broadmotion)
HDTV Upconversion – Let It Wave

- Breakthrough super-resolution Bandlet technology for HDTV upconversion
- Broadcasting equipment
  - Upconverter implemented on cost-effective Altera FPGA
    - Main features
      - Standard definition (SD) to high definition (HD) up to 1080P
      - 2-frame delay
      - Color conversion
      - Per pixel automatic film mode and cadence detection
      - Aspect ratio conversion
    - Additional features
      - Cross conversion 720P to 1080I
      - HD to SD down conversion
      - Video enhancement
    - Board reference design available
Video and Image Processing Suite
Baseline set of IP with standard interfaces and protocols that allow users to easily add their own proprietary algorithms

Optimized for Altera FPGAs

Works with any design flow
  - RTL, model-based design, C-based design
# Video and Image Processing Suite

<table>
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<tr>
<th>Core</th>
<th>Function</th>
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<tr>
<td>Deinterlacer</td>
<td>Converts interlaced video formats to progressive video format</td>
</tr>
<tr>
<td>Color space converter</td>
<td>Converts image data between a variety of different color spaces</td>
</tr>
<tr>
<td>Scaler</td>
<td>Resizes and clips image frames</td>
</tr>
<tr>
<td>Gamma corrector</td>
<td>Performs gamma correction on a color space</td>
</tr>
<tr>
<td>Alpha blending mixer</td>
<td>Mixes and blends multiple image streams, including picture-in-picture (PIP)</td>
</tr>
<tr>
<td>Chroma resampler</td>
<td>Changes the sampling rate of the chroma data for image frames</td>
</tr>
<tr>
<td>2D filter</td>
<td>Implements a 3x3, 5x5, or 7x7 finite impulse response (FIR) filter on an image data stream to smooth or sharpen images</td>
</tr>
<tr>
<td>2D median filter</td>
<td>Implements a 3x3, 5x5, or 7x7 filter that removes noise in an image by replacing each pixel value with the median of neighboring pixel values</td>
</tr>
<tr>
<td>Line buffer compiler</td>
<td>Efficiently maps image line buffers to Altera on-chip memory</td>
</tr>
</tbody>
</table>
2D Filtering

- 2D FIR filter and 2D median filter
  - 3x3, 5x5 or 7x7 filter sizes
- Useful for noise reduction and smoothing filters
- Supports symmetric optimization
Color Format Conversion

- Supplied as three separate cores
  - Color space converter
  - Chroma resampler
  - Gamma corrector

- Supports
  - RGB (computer and studio formats)
  - YIQ/YUV (NTSC, PAL, SECAM)
  - YCbCr (4:4:4, 4:2:2, 4:2:0)
Image Blending and Picture-in-Picture Mixing

- Multi-layer mixing (2 to 8 layers)
- Per-pixel alpha blending
- Run-time control of picture-in-picture location
Scaling

D1/SDTV: 720 x 480

- Supports standard-resolution conversions
- Nearest neighbor or bilinear filtering
- Clipping

HDTV 1080p: 1920 x 1080
Deinterlacing

- “Bob” and “Weave” supported

“Bob” – 1 Field

“Weave” – 2 Fields
Line Buffer Compiler

- Provides line buffers, making efficient use of FPGA internal memories
- Optimized for typical SD and HD resolutions
- Any number of bits per color plane
  - Choose line length, width, number of lines
Model-Based Design for Video Processing
Design Flow Starting with Model-Based Design

- **DSP Builder for data path**
  - Design
  - Simulation
  - Creation of an SOPC Builder component

- **SOPC Builder for system integration**
  - External RAM controllers
  - Sources and sinks
  - Processor integration
    - Nios® II or external processor

- **Compile in Quartus® II software**
Configure Blocks with GUI

- IP Toolbench
  - Launched from Quartus II software or directly in DSP Builder
DSP Builder Video Library

- Alpha blending mixer
- Chroma resampler
- Color space converter
- Gamma corrector
- Deinterlacer
- 2D FIR filter
- 2D median filter
- Scaler
SOPC Builder System Integration

DSP Builder Data Path

- Add
  - Sources
  - Sinks
  - Arbitrated DDR, SDR
  - Control

SOPC Builder System
Example 1: Single Input Video Channel

- Composite video input
- VGA output

Composite Video Input (NTSC) \(\rightarrow\) NTSC Interfaces

Deinterlacing \(\rightarrow\) Chroma Resampling \(\rightarrow\) Color Space Conversion (YCbCr \(\rightarrow\) RGB) \(\rightarrow\) Gamma Correction \(\rightarrow\) Scaling \(\rightarrow\) 2D 5x5 FIR Filter (Sharpening)

Nios II Processor

Static Image \(\rightarrow\) Picture-in-Picture Mixing \(\rightarrow\) Triple Buffer \(\rightarrow\) VGA Controller \(\rightarrow\) Video Output (VGA)

Data Interface

Control Interface
Example 2: Single Input Video Channel

- SDI video input/output

![Diagram of video channel processing pipeline]
Example 3: Multiple Video Channel Input

- Dual composite video input
- VGA output

Data Interface →
Avalon Control Interface →

Composite Video Input (NTSC)

NTSC Interface → Deinterlacing → Chroma Resampling → Color Space Conversion (YCbCr → RGB) → Gamma Correction → Scaling → 2D 5x5 FIR Filter (Sharpening)

Deinterlacing → Chroma Resampling → Color Space Conversion (YCbCr → RGB) → Gamma Correction → Scaling → 2D 5x5 FIR Filter (Sharpening)

Nios II Processor

Picture-in-Picture Mixing → Triple Buffer → VGA Controller → Video Output (VGA)

External Memory

Composite Video Input (NTSC)

NTSC Interface → Deinterlacing → Chroma Resampling → Color Space Conversion (YCbCr → RGB) → Gamma Correction → Scaling → 2D 5x5 FIR Filter (Sharpening)

Triple Buffer
Video and Image Processing (VIP) Example Design
Example of a Video System

- System block diagram
- DSP Builder
  - Implementation
  - Simulation
  - Conversion to HDL
- SOPC Builder integration
- Program hardware platform
VIP Upconversion System

- NTSC Video Input: Composite Input on Video Daughtercard
- Video Upconversion
- Triple Buffer
- HD Video Output: VGA Controller
- DDR II SDRAM
- DSP Builder

SOPC Builder
Video Upconversion Data Path

- Entire data path is assembled in DSP Builder

Deinterlacer MegaCore® → Chroma Resampler MegaCore → Color Space Converter MegaCore → Scaler MegaCore

- Two Avalon® Master Interfaces

640 x 480 Interlaced 60 Hz YCbCr 4:2:2
640 x 480 Progressive 30 Hz YCbCr 4:2:2
640 x 480 Progressive 30 Hz YCbCr 4:4:4
640 x 480 Progressive 30 Hz RGB
1,024 x 768 Progressive 30 Hz RGB
DSP Builder Implementation - Deinterlacer

Parameterize Deinterlacer

- Up to 1920 x 1080 Supported
- Bob and Weave Supported

Image Data Format:
- Image resolution: 640x480 Pixels
- Bits per pixel per color plane: 8 Bits
- Number of color planes in sequence: 2 Planes

Behavior:
- Deinterlacing method: Weave
- Base address of frame buffers: 0x11000000
DSP Builder Implementation: External Memory for Deinterlacer

Parameterize External Memory (Simulation-Only Model)
DSP Builder Implementation: Chroma Resampler

- Image resolution: 640x480
- Bits per pixel per color plane: 8
- Color Plane Configuration: Three color planes in sequence
- Conversion format: 4:2:2 to 4:4:4
- Horizontal interpolation: 2D Linear
- Vertical interpolation: 2D Linear

Cancel   Finish
DSP Builder Implementation: Color Space Converter

Parameterize - Color Space Converter MegaCore Function

Image Data Format:
- Image resolution: 640x480 Pixels
- Bits per pixel per color plane: 8 Bits

Color Plane Configuration:
- Three color planes in sequence
- Three color planes in parallel

Precision:
- Word length: 18 Bits
- Integer part of word length: 11 Bits
- Fractional part of word length: 7 Bits
- Overflow behavior: Saturate
- Underflow behavior: Saturate

Compile Time Coefficients:
- Color model conversion: Y’CbCr 3Dy to Computer RGB
- Din and dout refer to the input and output channels respectively.
- dout_0 = 1.164, *dn_0 + 0 *dn_1 + 1.596 *dn_2 + 222.012
- dout_1 = 1.164, *dn_0 + 0.361 *dn_1 + 0.013 *dn_2 + 135.488
- dout_2 = 1.164, *dn_0 + 2.018 *dn_1 + 0 *dn_2 + 276.028

Finish
DSP Builder Implementation: Scaler
DSP Builder Implementation:
Libraries Generated

Deinterlacer

External Memory (Simulation)

Color Space Converter

Chroma Resampler

Scaler
DSP Builder Implementation: Connecting Functions

Connecting library functions is simple due to standard interface and protocol.

Connections Between the Color Space Converter and Scaler
Simulation: Video Input
Simulation: Generate Video Binary File

- Command Line Utility converts AVI file to a binary file for use within DSP Builder environment
- Also converts binary output to an AVI file for convenient playback

```
Command Prompt
C:\data\VIP\Video_IP_Example_Design\avi-is-avi>avi-is-avi
Incorrect number of arguments specified

Terminating
Version 0.14
Usage: avi-is-avi "InputFile" "OutputFile" IS_width IS_height mode\AVITOIS\ISToAVI

Optional Parameters:
-v Enable Video viewers
-c IS colourspace \{RGB\|YCbCr\} default YCbCr
-s IS subsampling \{444\|422\|420\} default 444/0ff
-q IS channels in sequence \{0\|1\} default 3
-\i Enable IS interlace
-\b Begin frame number default 0
-\e End Frame number default -1 \(\text{runs to end}\)
-\p Frame advance default 1
-r Output AVI fps default 15

* Only used \AVItoIS\ mode
** Only used \ISToAVI\ mode
```

C:\data\VIP\Video_IP_Example_Design\avi-is-avi>
Simulation: Video Output

1. Image Stream Sink

2. Block Diagram

3. Schematic Diagram

4. Binary File Writer
Simulation: Upconversion Subsystem
Convert to VHDL: Signal Compiler
Top-Level Design File in Quartus II
System Integration: SOPC Builder

DSP Builder - Data Path
- NTSC
- BT.656
- Buffer
- VGA Out
- DDR2
Custom Hardware

- Generated custom video interfaces IP
  - Available within reference design package
NTSC Video Input

- Video data capture with TI TVP5146 decoder
  - I2C is control interface for device configuration

- Controller designed in HDL
  - Imported into SOPC Builder
Triple Buffer and VGA Output

- Allows inputs and output to run asynchronously and at different frame rates
  - Video output: 1,024 x 768 progressive at 30 frame/s
  - VGA output: must run at least 60 fps

- HDL design, imported into SOPC Builder
Video Development Kit, Cyclone II Edition

- Device: EP2C70
- Bundled software:
  - Quartus II development kit edition
  - DSP Builder
  - MATLAB/Simulink evaluation software
  - Altera OpenCore® Plus evaluation IP
- Includes video input daughter card
Video Input Daughter Card

- Dual composite video inputs (NTSC & PAL)
- Compatible with other Altera development boards that feature a Santa Cruz connector
Download to Hardware

- Resource utilization
  - 9,500 logic elements, 48 M4K, 11 multipliers
  - Fits in EP2C15 device

- Program Video Development Kit, Cyclone II Edition

- Hardware debug
  - JTAG/SignalTap® logic analyzer
Getting Started
Altera Video Solutions

Design Software

Support Tools

Intellectual Property (IP)

Development Kits

Video Processing

Partner IP and Design Services

Video Dev. Kits
- Daughter Card $195
- Cyclone II $1,095
- Stratix II GX $4,995

Altera Training

DSP Builder SOPC Builder

Video IP Suite $995

Reference Designs

SOPC World

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Audio Video Development Kit, Stratix II GX Edition

- Device: EP2SGX90
- Video interfaces:
  - 4 SDI/HD-SDI channels
  - DVI
- Audio interfaces:
  - AES3/EBU, SPDIF
- High-speed data interfaces:
  - ASI
  - FireWire (IEEE1394)
  - USB 2.0
  - 10/100/1000 Ethernet
- Bundled with SDI and video processing reference design
## Get Started Now

<table>
<thead>
<tr>
<th>Product</th>
<th>Description</th>
<th>Ordering Code</th>
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<tbody>
<tr>
<td>Video and Image Processing Suite</td>
<td>9 video and image processing IP cores</td>
<td>IPS-VIDEO</td>
<td>$995</td>
</tr>
<tr>
<td>Video Development Kit, Cyclone II Edition</td>
<td>Cyclone II DSP board + video input daughtercard</td>
<td>DK-VIDEO-2C70N</td>
<td>$1,095</td>
</tr>
<tr>
<td>Video Input Daughter Card</td>
<td>2 composite video inputs (NTSC/PAL Support)</td>
<td>DC-VIDEO-TVP5146N</td>
<td>$195</td>
</tr>
<tr>
<td>Audio Video Development Kit, Stratix II GX Edition</td>
<td>Stratix II GX video board with ASI, SDI, DVI, Gigabit Ethernet, FireWire, USB2.0, S/PDIF, AES</td>
<td>DK-VIDEO-2SGX90N</td>
<td>$4,995</td>
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Thank You
Q & A