Designing Video Surveillance Equipment Using Altera and TI Technology
Agenda

- Digital video recorder (DVR) market and technical overview
- Key system diagrams
- Altera solutions for DVR application
  - Video intellectual property (IP) library suite
  - Video compression IP
  - Interface IP
- Altera and Texas Instruments (TI) solution for DVR applications
- Development kit
DVR Market and Technical Overview
DVR Market Dynamics

- Strong growth expected
  - Increasing public security consciousness
  - Updating old analog systems
  - Extending into new vertical markets (e.g., banking, retail, roads, prison)

- Asia Pacific manufacturers are playing important role
  - Lower price wins the market share
  - Increased investment in R&D
System Revenue Forecasts

Source: Frost & Sullivan 2005
Technical Trends

- New compression algorithm improve video quality and saves storage space
  - M-JPEG to MPEG4 to H.264

- Increasing number of IP-based systems
  - Distributed capture and centralized storage
  - IP-based camera and IP video server
  - Network DVR

- Further improvements on intelligent image analysis and accurate video motion detection algorithm
IP Network Video Surveillance System
System Diagram
Typical Platforms

- Hardware compression DVR system
  - Embedded DVR (stand-alone)
  - PC/IPC-based DVR system

- Software compression DVR system
  - PC/IPC-based system

- Video server

- IP camera

- Network DVR
DVR System: Hardware Compression

- Video Decoder
- Video QUAD/Multiplexer Controller
- Multi-Channel Video Decoder
- PCR or H.264 Hardware Compression
- CPU (Nios® Processor)
- Embedded DVR
- Ethernet
- Video Server and Network DVR
- PC-Based DVR
- SDRAM
- Altera FPGA
- IDE or SATA
- Audio ADC
- CCIR656
- I2S

4/9/16 Channels
PCI Based DVR: PC Software Compression

Channels

Audio ADC

SDRAM

Video Decoder

CCIR656

H/V Scalar

FIFO

DMA Controller

DMA Controller

PCI or PCI Express Bridge

PCI Bus

Altera FPGA
Other Key Functions:
- PIP
- Overlay or Blending
Altera Video Surveillance Solutions

- Video compression algorithms
- Video IP library and imaging reference design
- Memory controller and bus interfaces
- Development kits
- Digital signal processing (DSP) system and FPGA design tools/utilities (see demo area)
Altera Video Compression Solutions
Choosing the Compression

<table>
<thead>
<tr>
<th>Feature</th>
<th>M-JPEG</th>
<th>M-JPEG2000</th>
<th>H.264</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compression</td>
<td>10-20</td>
<td>10-20</td>
<td>25-50</td>
</tr>
<tr>
<td>Bit Rate (Mbps)</td>
<td>6-12.5</td>
<td>6-12.5</td>
<td>2.5-5</td>
</tr>
<tr>
<td>Motion Compensation</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Variable Bit Rate (VBR)</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Constant Bit Rate (CBR)</td>
<td>No</td>
<td>Yes (Instant Tier 2)</td>
<td>Yes (Buffered)</td>
</tr>
<tr>
<td>Latency</td>
<td>Low</td>
<td>Low to Medium</td>
<td>Medium to High</td>
</tr>
<tr>
<td>Blocking Artifacts</td>
<td>Yes</td>
<td>No (Full Frame)</td>
<td>Yes</td>
</tr>
<tr>
<td>Lossless Support</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>RGB Support</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Stream Scalability</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Relative Cost</td>
<td>1x</td>
<td>3x</td>
<td>2x</td>
</tr>
</tbody>
</table>

Note: MPEG-4 AVC (Main Profile)
- Higher Compression
- Higher Complexity (3-4x)
Case Study: Video Surveillance Using Cyclone® II FPGAs

D1 Resolution

Video In → Video ADC → FPGA → Memory → HDD

Video Digital Access Card (DAC) → Video Out

Stream → ENET PHY
## Video Surveillance Building Blocks

<table>
<thead>
<tr>
<th>System</th>
<th>File System</th>
<th>RTP/UDP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Video Processing</td>
<td>De-interlacing</td>
<td>Scaling</td>
</tr>
<tr>
<td>Video Compression</td>
<td>M-JPEG</td>
<td>M-JPEG2000</td>
</tr>
<tr>
<td>Video Interfaces</td>
<td>BT-656</td>
<td>SD-SDI</td>
</tr>
<tr>
<td>Interfaces</td>
<td>I²S</td>
<td>I²C</td>
</tr>
</tbody>
</table>

| Hardware | Software |
Complexity Analysis: Logic

Applicable for real-time full D1 processing
Complexity Analysis: Memory

- JP2K Max. M4K
- JP2K Min. M4K
- H.264 Max. M4K
- H.264 Min. M4K
- JPEG Max. M4K
- JPEG Min. M4K
- Cyclone II Devices

Applicable for real-time full D1 processing

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M-JPEG System

YUYV… 4:2:2 → Raw to Block Conversion → JPEG Encoder → EMAC → RFC2435 to PHY

- 300 LEs
- 23 M4Ks
- 8,900 LEs
- 18 M4Ks
- 2,500 LEs
- 2,000 LEs

* 4:2:0 is also possible.
MPEG-4 Simple Profile System

- RAW to Block Conversion (YUYV... 4:2:2) 300 LEs
- SDRAM Controller 2,000 LEs
- MPEG-4 Encoder 18,000 LEs 92 M4Ks
- Buffered Reference Frame
- NiosII 2,500 LEs
- RTP - System Init.
- EMAC 2,000 LEs
- RFC3016 to PHY

31 Mbps

DDR SDRAM

Y Y Y U V

4:2:0
M-JPEG2000 System

- Buffered color planes
- Buffered transformed tile
- Buffered coding passes

SDRAM Controller

- 31 Mbps
- (81 Mbps)
- 19 Mbps

22,000 LEs
165 M4Ks (4:2:0)

YUYV… 4:2:2
RGB...

Color Plane Buffer and Tiler

JPEG2000 Encoder

Hardware Tier 2 (CBR)

Nios II

2,500 LEs

RTP
System Init.

IETF (Draft) to PHY

4,000 LEs

2,000 LEs

DDR SDRAM

SDRAM Controller

EMAC

2,500 LEs

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## Case Study Summary

<table>
<thead>
<tr>
<th>Requirement</th>
<th>M-JPEG</th>
<th>MPEG-4 SP</th>
<th>M-JPEG2000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Components:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>− Raw to Block</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>− Encoder</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>− SDRAM Controller</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>− Ethernet MAC</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>− Nios II Processor</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>LEs</td>
<td>14,000</td>
<td>23,000</td>
<td>32,500</td>
</tr>
<tr>
<td>M4Ks</td>
<td>52</td>
<td>105</td>
<td>183</td>
</tr>
<tr>
<td>SDRAM Bandwidth</td>
<td>0</td>
<td>62 Mbps*</td>
<td>131 Mbps</td>
</tr>
<tr>
<td>Cyclone II</td>
<td>EP2C20C8</td>
<td>EP2C35C8**</td>
<td>EP2C70C8</td>
</tr>
<tr>
<td>Frequency</td>
<td>16 MHz</td>
<td>100 MHz</td>
<td>80 MHz</td>
</tr>
</tbody>
</table>

• Reducing the Bandwidth Is Possible by Using M4Ks for Raw to Block Conversion

** $25 Volume Price
H.264 Video Encoding
H.264 Video Compression

- JPEG, JPEG2000, MPEG-2, H.263, MPEG-4 part 2, MPEG-4 part 10/H.264 AVC all used in security/surveillance industry

- H.264 compression rates = 2x faster than competing standards at comparable quality

- Penalty is that H.264 encoding is extremely computationally intensive
FPGAs Are Ideal for H.264

- MPEG4-AVC is heavily computing-hungry
  - Processor limited by internal architecture (with 8 internal multipliers, can perform 8 multiplications per cycle)
    - TI DM6446 DSP requires 1-GHz clock for standard definition (SD) 30-fps encode
  - FPGA is highly scalable, supports 100 multiplications per cycle

- Tasks parallelization is mandatory
  - Several processors needed to process picture slices, easier to compute
  - FPGA can process bulk picture or larger slices
H.264 Solution #1

- Primary lead provider: CAST
  - Right performance level for VS
    - Baseline, SD/D1 at 30 fps
  - Available today
    - Encoder, decoder, multi-channel encoder
  - Efficient implementation
    - ~20K LEs
  - Existing Altera customer engagements
H.264 Solution #2

- New partner: 4i2i
  - Right performance level for VS
    - Baseline, reference design = 3x [SD + common intermediate format (CIF)] at 30 fps
  - Available today
    - CODEC, multi-channel
  - Efficient implementation
  - DVR reference design in debug
Altera Video IP Functions
Altera Video and Imaging IP Library Suite

- Library of common video and image processing functions
  - Baseline set of IP with standard interfaces and protocols that allow users and third parties to easily add their own proprietary algorithms
  - Works with any design flow
    - RTL, model-based design, or C-based design
  - Reference design and development kit available

- IP cores optimized for Altera FPGAs
  - 2D digital filters: finite impulse response (FIR), median
  - Color space conversion
  - Image mixing/blending
  - Scalar (vertical/horizontal)
  - Deinterlacer
  - 2D fast Fourier transform (FFT)
  - Video buffer compiler

*Altera Ordering Code: IPS-VIDEO*
2D FIR Filter and 2D Median Filter

- Support 3x3 pixel, 5x5, and 7x7 kernel sizes
  - Support 9x9, 11x11, 13x13 in future releases
- Support 8-bit, 10-bit, and 16-bit pixel input data
- Configurable support for handling image edges
- Optimized for FPGA architecture
Color Space Converter

- Color spaces supported:
  - RGB (computer and studio formats)
  - YIQ/YUV (NTSC, PAL, SECAM)
  - YCbCr (4:4:4, 4:2:2, 4:2:0) with chroma resampling
    - Support pixel replication/decimation
    - Support bilinear interpolation
    - Support bicubic interpolation
  - CMYK (document imaging)
  - Bayer conversion (CCD/CMOS sensor format) demosaic

- Supports gamma correction
Image Blending and Picture-in-Picture Mixing

- Supports 8-bit and 10-bit pixel data
- Supports OpenGL texturing standards, i.e., RGBA2, RGBA4
- Alpha blending on pixel-by-pixel basis
- Multiple color plane mixing (2 to 8 layers)
- Run-time control of picture-in-picture location
- Supports full-screen high-definition (HD) graphics
Image Scaling

- Independent scaling for vertical/horizontal with arbitrary scaling ratios
- Choice of filtering techniques
  - Linear (2-tap, 8-phase polyphase filter per dimension implementation)
  - Higher order interpolation (8-tap, 32-phase polyphase filter per dimension)
- Support 8-bit and 10-bit pixel input data and image clipping

D1/SDTV: 720x480

HDTV 1080p: 1920x1080
Deinterlacing Options

- Bob and weave techniques: available in first release
- Motion adaptive deinterlacing: available in first release
  - “Weave” for still areas of the picture, “bob” for areas of motion
- Motion compensated deinterlacing: available in future release
2D Fast Fourier Transform (FFT)

- Supports discrete set of transform sizes
  - 64x64, 256x256, 1024x1024
- Supports both fixed point and floating point
- Supports up to 16-bit pixel input data
Video Buffer Compiler

- Allows efficient use of FPGA internal memories to store line buffers
- Optimized for typical SD and HD resolutions
- Supports Stratix® II and Cyclone II memory architectures
- Supports 8-bit and 10-bit pixel input data
Altera Memory Controller and Bus Interface Solutions
PCI/PCI-Express in DVR System

- More than 70% DVR systems based on PCI and PCI Express interface
- Next-generation system will be based on PCI Express
  - Standard configuration for PC
  - PCI bandwidth limitation for multi-channel video
- Altera offers complete solution for PCI and PCI Express interfaces
Altera PCI Express Solutions

- Complete, easy-to-use PCI Express solutions
  - x1, x4 & x8 endpoints
  - Industry-leading design flow with Altera MegaCore® IP
  - Stratix II GX, Cyclone II, Stratix II, HardCopy® II and Stratix GX device support

- Low-risk, hardware-verified solutions
  - PCI-SIG-compliant and device characterization
  - 2 generations of FPGAs with embedded transceivers
    - Stratix GX passed PCI-SIG compliance
    - Stratix II GX targeting PCI-SIG compliance May 2006
  - Development/demonstration boards

Fastest Time-to-Market with a Reliable PCI Express Endpoint Solution
# FPGAs and Options Supported

<table>
<thead>
<tr>
<th>Feature</th>
<th>x1</th>
<th>x4</th>
<th>x8</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Device Family Support</strong></td>
<td>Stratix II GX</td>
<td>Stratix II GX</td>
<td>Stratix II GX</td>
</tr>
<tr>
<td></td>
<td>Stratix II</td>
<td>Stratix II</td>
<td>Stratix II</td>
</tr>
<tr>
<td></td>
<td>Cyclone II</td>
<td>Cyclone II</td>
<td>Cyclone II</td>
</tr>
<tr>
<td></td>
<td>Stratix GX</td>
<td>Stratix GX</td>
<td>Stratix GX</td>
</tr>
<tr>
<td><strong>Virtual Channels</strong></td>
<td>1 to 4</td>
<td>1 to 4</td>
<td>1 or 2</td>
</tr>
<tr>
<td><strong>Advanced Error Reporting (AER)</strong></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td><strong>End-to-End Cyclical Redundancy Check (ECRC)</strong></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td><strong>Data Path Width</strong></td>
<td>64 bits</td>
<td>64 bits</td>
<td>64 bits</td>
</tr>
<tr>
<td><strong>Frequency of Operation ($f_{\text{MAX}}$)</strong></td>
<td>62.5 MHz, 125 MHz</td>
<td>125 MHz</td>
<td>250 MHz</td>
</tr>
</tbody>
</table>
Other IP Cores Available

- Ethernet MAC, I²C, SATA
- Various memory controllers
  - DDR, DDR2, RLDRAM II
Altera and TI Solution
## Cost Challenge

3 D1 Channels + 3 CIF Channels + Analytics + Video Streaming

<table>
<thead>
<tr>
<th></th>
<th>DSP-Only Solution</th>
<th>FPGA+DSP Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA</td>
<td>None</td>
<td>2C50</td>
</tr>
<tr>
<td>DSP</td>
<td>6 DM6446</td>
<td>DM642 (Analytics)</td>
</tr>
<tr>
<td>Memory</td>
<td>3 DDR2 SDRAM</td>
<td>1 DDR2 SDRAM</td>
</tr>
<tr>
<td>Total Silicon Cost</td>
<td>$195</td>
<td>$60</td>
</tr>
</tbody>
</table>

Too High
Why Use FPGAs and DSPs

- DSPs yield quick implementation of core processing
- FPGAs add specialized parallel-processing optimizations where serial instruction sets of DSPs fail
- Migrate suitable algorithms from DSP to FPGA coprocessor over time
DVR Architecture Proposal #1

Advantages:
- Front-end analytics
- Streaming capability

Disadvantages:
- Cost
- 2-chip solution

Diagram:
- DDR2
- TI DSP DM642
- D1 Video Channel 1
- D1 Video Channel 2
- D1 Video Channel 3
- Video Capture Analytics
- Video Streaming
- Ethernet
- FPGA EP2C70
- H.264 D1 + CIF Encode

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DVR Architecture Proposal #2

Advantages:
Cost
Scalable to $n$ channels

Disadvantages:
Limited analytics
Multi-chip solution

SD Video Channel 1
TI A/D
FPGA
- Ethernet MAC IP $n \times$
- Nios II 32-bit microcontroller
- H.264 D1 + CIF encode

SD Video Channel 2
TI A/D
SD Video Channel n
TI A/D

DDR2

Ethernet PHY

Ethernet

TI A/D
Development Kits
Cyclone II Video Development Kit

- **FPGA density**
  - EP2C35 to EP2C70
  - EMIF connector to TI DSP kits

- **Video capture/input daughter card**
  - Dual inputs
  - Composite video (NTSC/PAL)
  - *Also compatible with Stratix II DSP Kits*

- **Bundled software**
  - Quartus® II (FPGA design)
  - DSP Builder (DSP design)
  - Matlab/Simulink evaluation
  - VIP Suite evaluation
  - IP cores

*Altera eStore On-Line Ordering Code = DK-VIDEO-2C70N (shown above) or DSP-DEVKIT-2C35 + DC-VIDEO-TVP5146N*
Sendero Board PCI Express

PHILIPS USB 2.0 Controller

Altera EPM240T100C5

ISSI 4-Mbyte SRAM

64-Mbyte FLASH

Extension Headers

ISSI 36-Mbyte QDR SRAM

ISSI 256-Mbyte DDR SDRAM

Altera EP2C35F672C6

DVI In

DVI Out

Ordering Information:

Stratix II GX Audio/Video Development Kit

- FPGA density
  - EP2SGX90
- Video
  - Digital video interface (DVI) inputs/outputs
  - Four SD HD SDI inputs/outputs, including dual-link SDI support
  - Asynchronous Serial Interface (ASI) inputs/outputs
- Audio
  - AES3
  - Sony/Phillips digital interface (S/PDIF)
- Bundled software
  - Quartus II (FPGA design)
  - DSP Builder (DSP design)
  - Matlab/Simulink Evaluation
  - SDI reference design
  - VIP suite evaluation
  - IP cores

Altera eStore On-Line Ordering Code = DK-VIDEO-2SGX90N (shown above)
Other Development Kit Options

- Other video daughter cards:
  - ASI/SDI with 2C5 daughter card
  - Audio IO daughter card

- Cyclone III FPGA video development kit
  - In planning phase (contact Altera for schedule)
  - Will cover various applications, from video surveillance to consumer AV
Thank You
Q & A