

nbit_adder: adder1

GENERIC MAP (x => 8)

PORT MAP (AddSubR_n => M

multiplexer: mux2to3

GENERIC MAP (x => 16)

PORT MAP (A => Z, S => G

AddSubR_n <= (OTHERS => AddSubR

YOR AddSubR_n

YOR AddSubR_n

YOR AddSubR_n

YOR AddSubR_n

YOR AddSubR_n

YOR AddSubR_n

YOR AddSubR_n

YOR AddSubR_n

YOR AddSubR_n

YOR AddSubR_n

YOR AddSubR_n

YOR AddSubR_n

YOR AddSubR_n

YOR AddSubR_n

YOR AddSubR_n

YOR AddSubR_n

YOR AddSubR_n

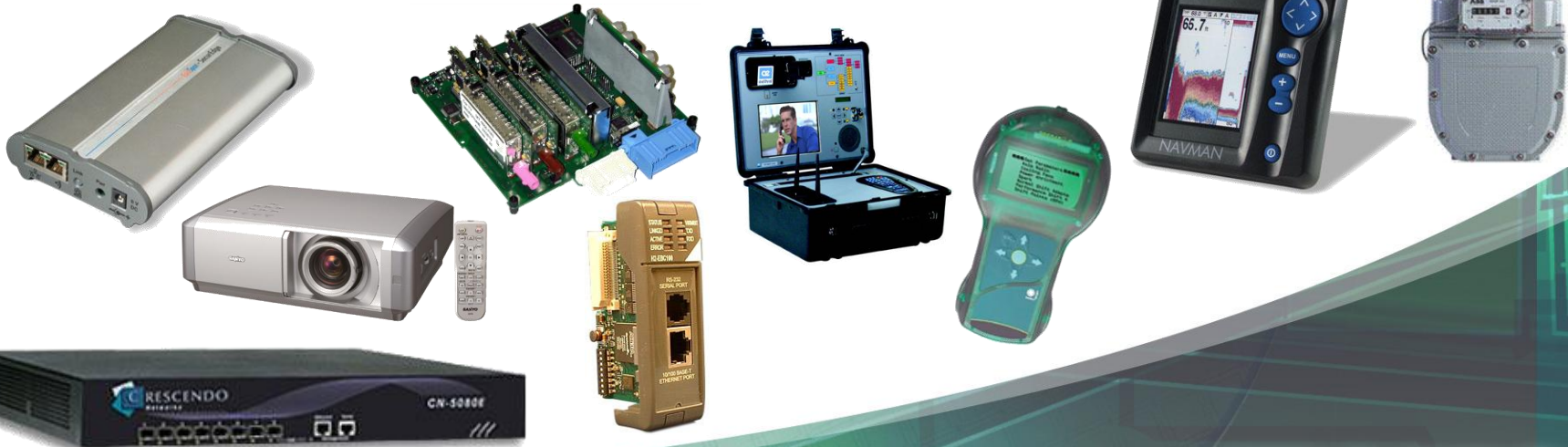
YOR AddSubR_n

YOR AddSubR_n

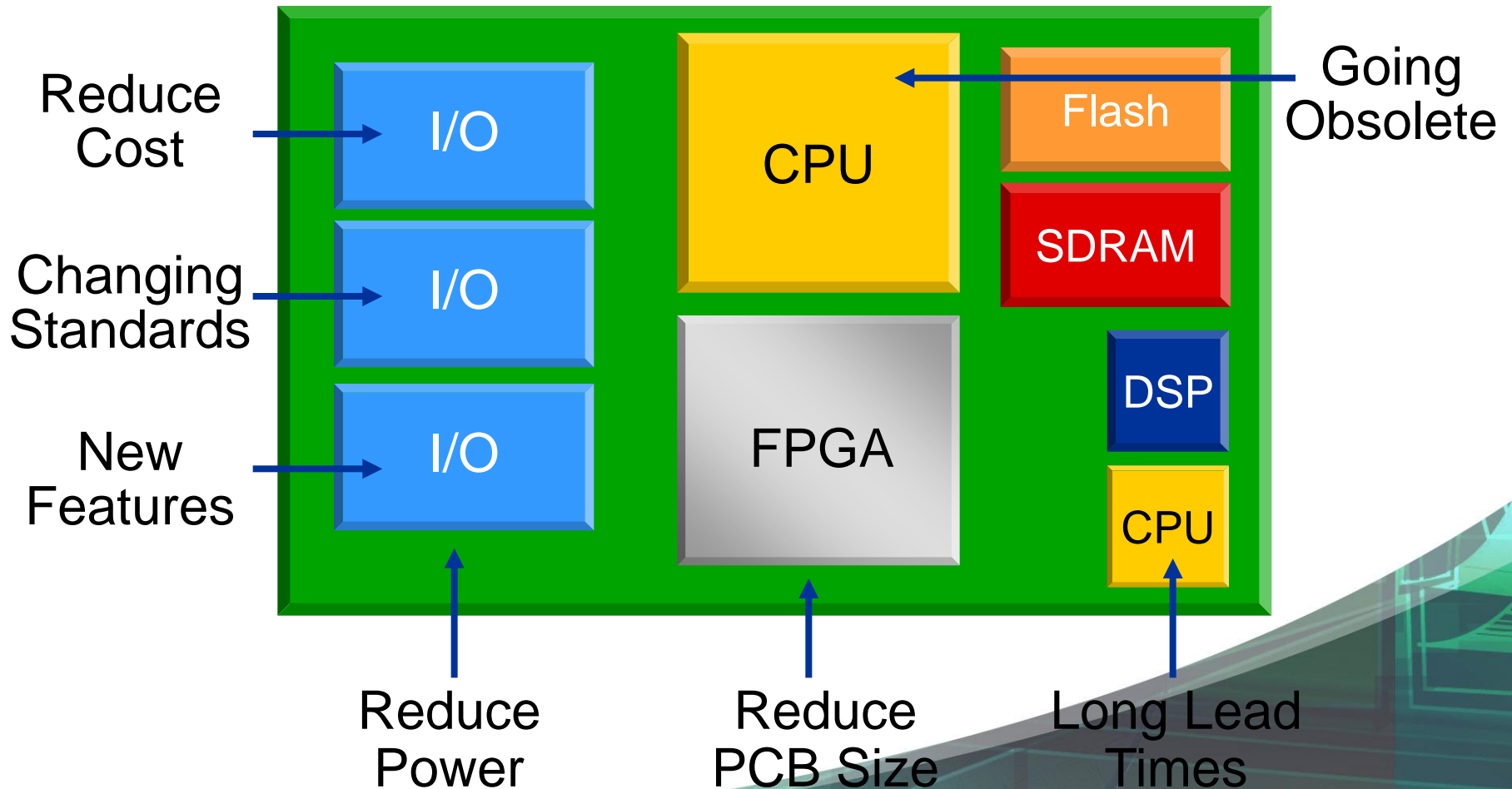
Implement System-on-a-Programmable Chip (SOPC) Designs in Minutes

The Embedded Revolution

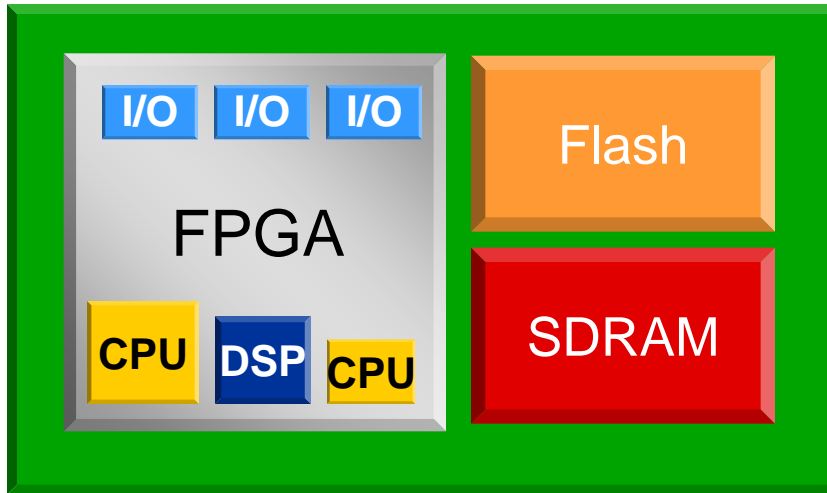
- FPGAs offer a new way to develop embedded systems
- Widely adopted:
 - Over 15,000 development kits shipped
 - Many products already in the market



Embedded Design Challenges



FPGA-Based Solution

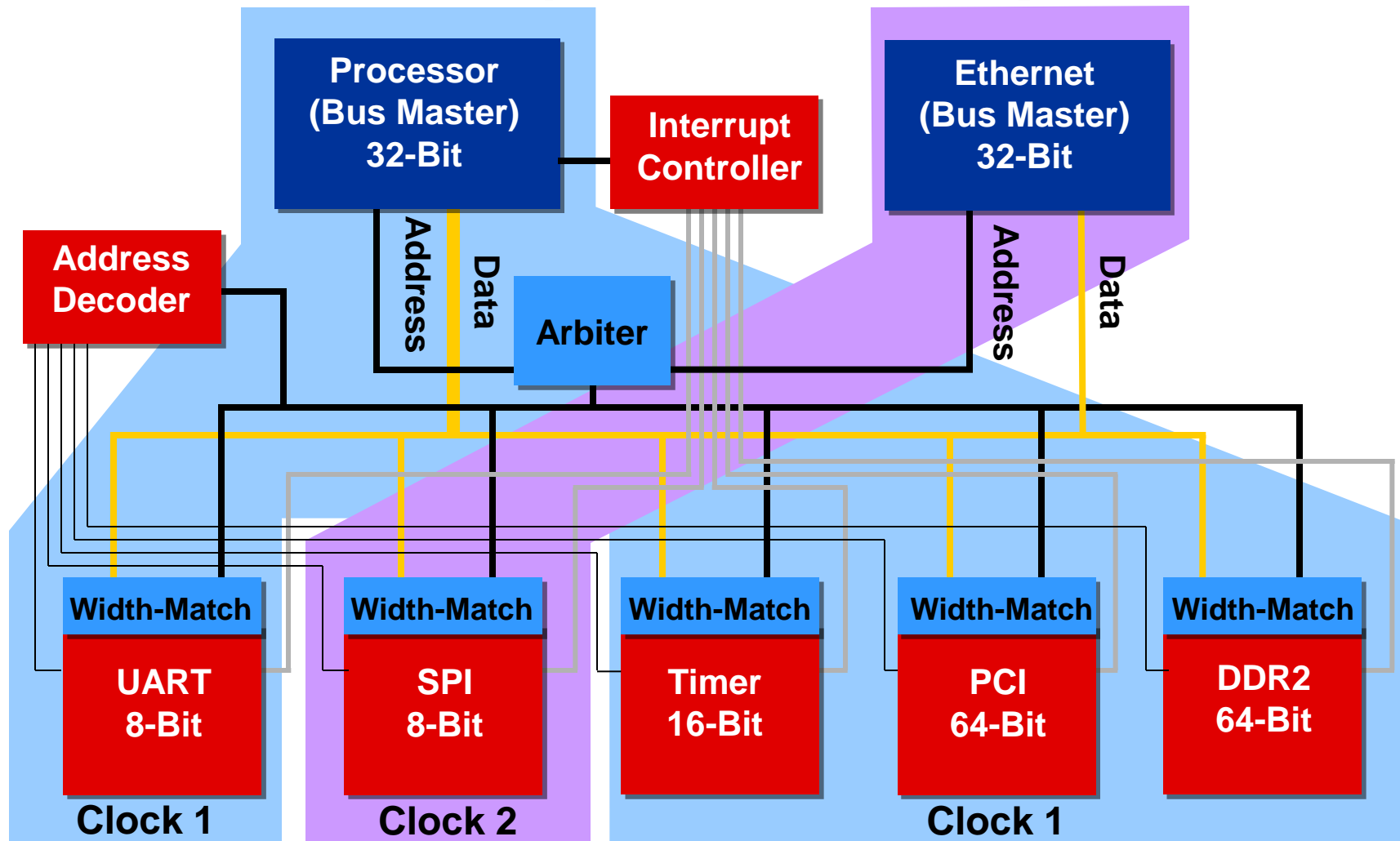


- Reduced power
- Reduced cost
- Reduced PCB size
- Easier to support
- Add new features
- Smaller B.O.M.
- Obsolescence protected



System Level Integration
**Replace External Devices
with Programmable Logic**

Traditional System Design

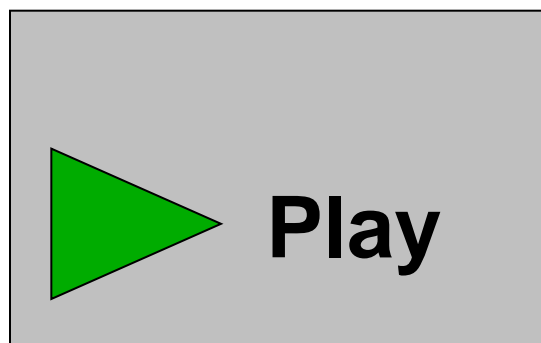


Large Amount of Complexity

What If...

Processor
(Bus Master)
32-Bit

Ethernet
(Bus Master)
32-Bit



UART
8-Bit

SPI
8-Bit

Timer
16-Bit

PCI
64-Bit

DDR2
64-Bit

What If...

Processor
(Bus Master)
32-Bit

Ethernet
(Bus Master)
32-Bit

Automated System
Integration Generator

Done!

UART
8-Bit

SPI
8-Bit

Timer
16-Bit

PCI
64-Bit

DDR2
64-Bit

Basic Integration

- Bus width matching
- Address decoding
- Interrupt controller

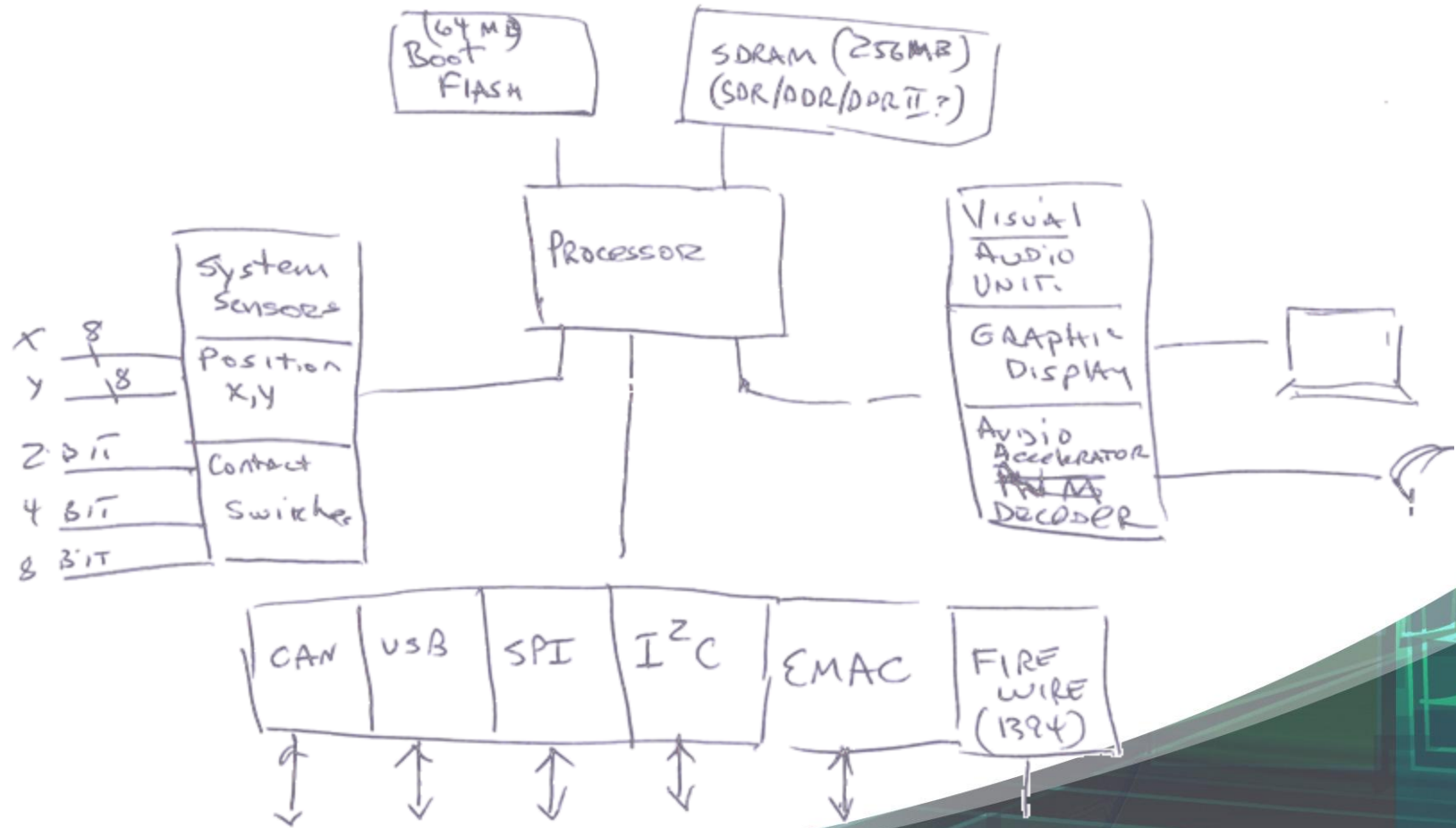
Advanced Tasks

- Arbitration logic
- Clock domain crossing
- Burst transfers

Optimization

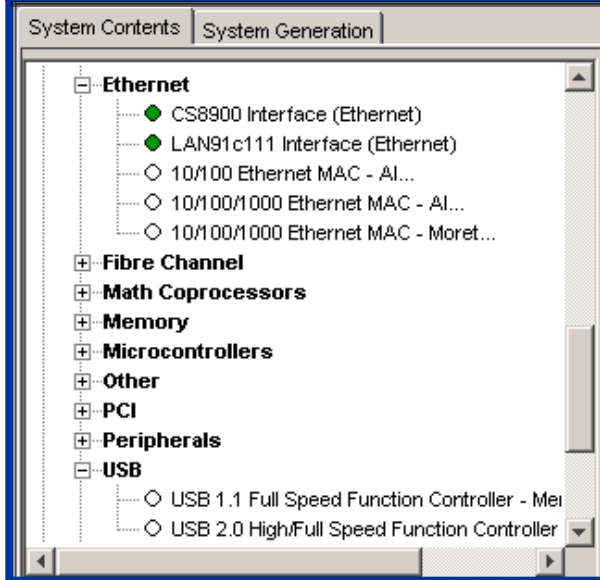
- System throughput
- Resource utilization

System Concept



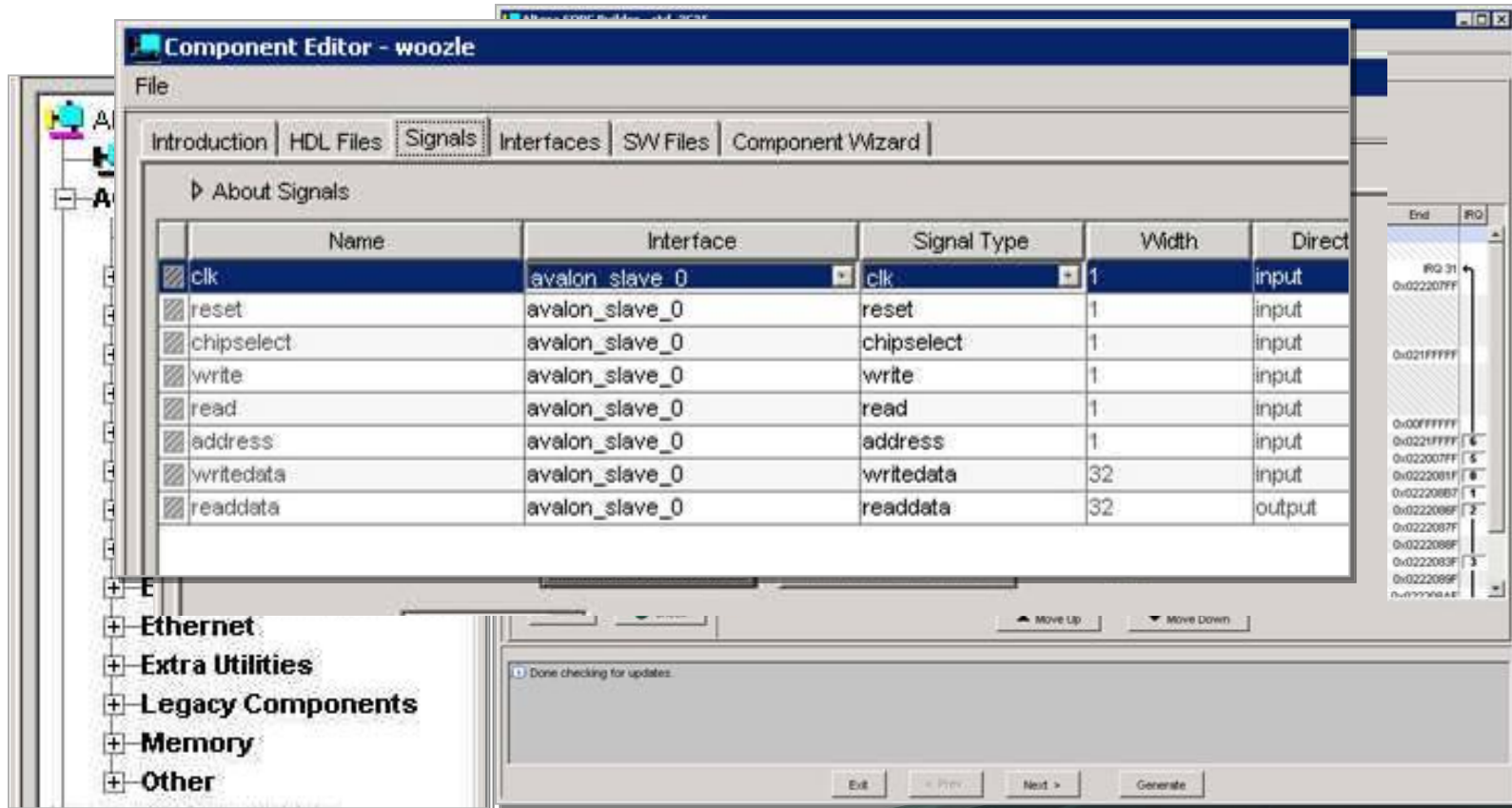
Design Flow

1. Select Intellectual Property (IP)



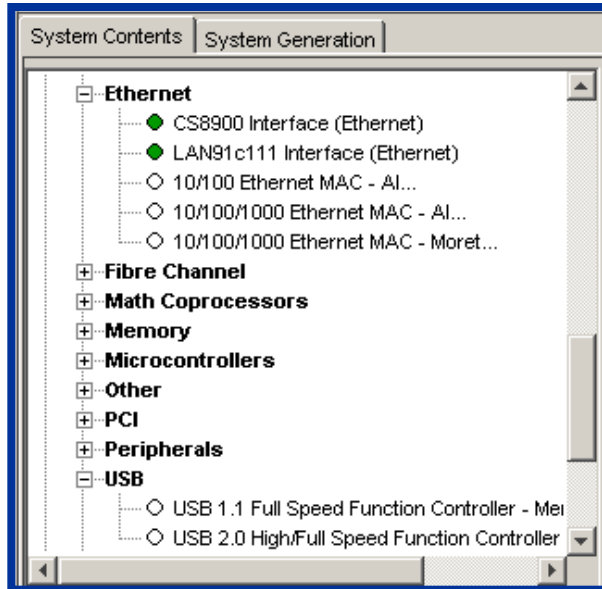
Component Selection

- Extensive portfolio of system components
- Component editor imports user-designed functions

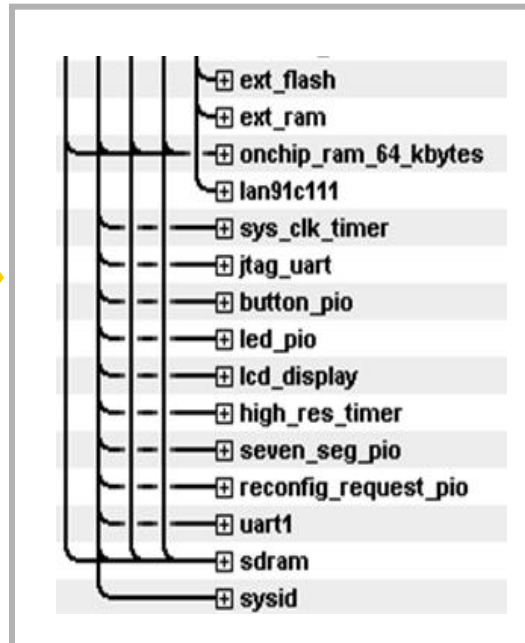


Design Flow

1. Select IP



2. Select Connections



System Editor

Connection Panel

Clock Domains

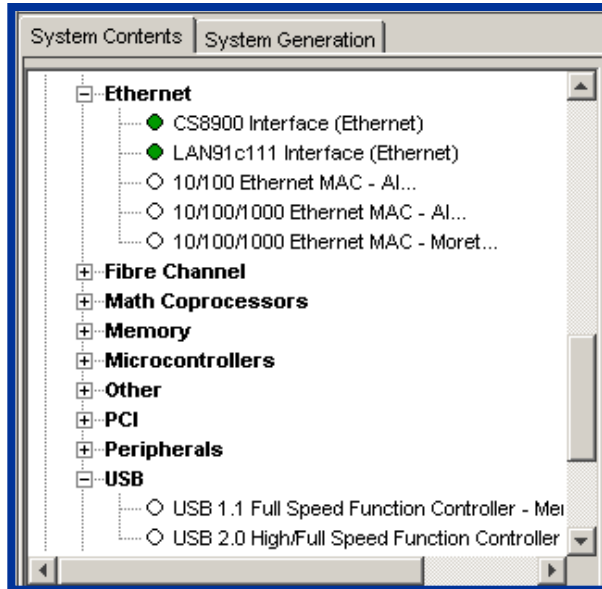
Address Map

Interrupt Controller (IRQ) Priorities

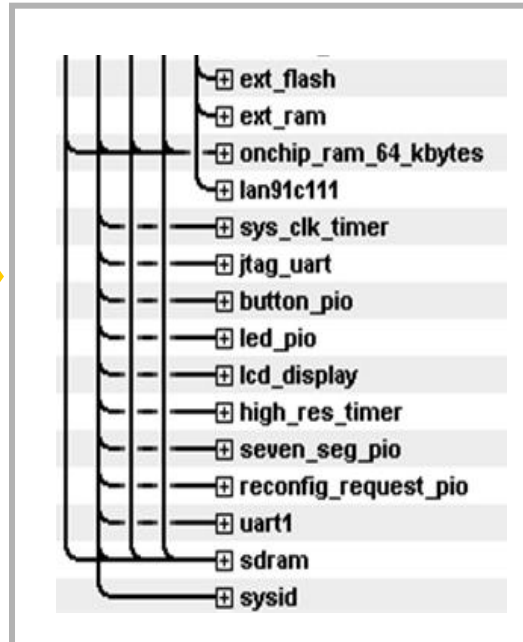
Use	Module Name	Description	Clock	Base	End	IRQ
<input checked="" type="checkbox"/>	cpu	Nios II Processor - Altera Corpora...	clk_85			
	instruction_master	Master port				
	data_master	Master port				
	jtag_debug_module	Slave port				
<input checked="" type="checkbox"/>	ext_ssram_bus	Avalon Tri-State Bridge	clk_85			
	avalon_slave	Slave port				
	tristate_master	Master port				
<input checked="" type="checkbox"/>	ext_ssram	Cypress CY7C1380C SSRAM		0x02000000	0x021FFFFFF	
<input checked="" type="checkbox"/>	ext_flash_enet_bus	Avalon Tri-State Bridge	clk_85			
	avalon_slave	Slave port				
	tristate_master	Master port				
<input checked="" type="checkbox"/>	ext_flash	Flash Memory (Common Flash Int...		0x00000000	0x00FFFFFF	
<input checked="" type="checkbox"/>	lan91c111	LAN91c111 Interface (Ethernet)		0x02210000	0x0221FFFF	6
<input checked="" type="checkbox"/>	epcs_controller	EPCS Serial Flash Controller	clk_85	0x02200000	0x0222007F	5
<input checked="" type="checkbox"/>	sys_clk_timer	Interval timer	clk_85	0x02220800	0x0222081F	0
<input checked="" type="checkbox"/>	jtag_uart	JTAG UART	clk_85	0x022208B0	0x022208B7	1
<input checked="" type="checkbox"/>	button_pio	PIO (Parallel I/O)	clk_85	0x02220860	0x0222086F	2
<input checked="" type="checkbox"/>	led_pio	PIO (Parallel I/O)	clk_85	0x02220870	0x0222087F	
<input checked="" type="checkbox"/>	lcd_display	Character LCD (16x2, Optrex 162...	clk_85	0x02220880	0x0222088F	
<input checked="" type="checkbox"/>	high_res_timer	Interval timer	clk_85	0x02220820	0x0222083F	3
<input checked="" type="checkbox"/>	seven_seg_pio	PIO (Parallel I/O)	clk_85	0x02220890	0x0222089F	
<input checked="" type="checkbox"/>	reconfig_request_pio	PIO (Parallel I/O)	clk_85	0x022208A0	0x022208AF	

Design Flow

1. Select IP



2. Select Connections



3. Generate System



Integrated Hardware/Software Flow

Use	Module Name	Clock	Base	End	IRQ	IRQ
<input checked="" type="checkbox"/>	cpu_0	clk	0x00000000	0x000007FF		
<input checked="" type="checkbox"/>	cpu0_memory	clk	0x00001000	0x00001FFF		
<input checked="" type="checkbox"/>	dma_0	clk	0x00000800	0x0000081F	0	
<input checked="" type="checkbox"/>	cpu_1	clk	0x00000000	0x000007FF		
<input checked="" type="checkbox"/>	cpu1_memory	clk	0x00002000	0x00002FFF		
<input checked="" type="checkbox"/>	dma_1	clk	0x000008C0	0x000008DF	7	
<input checked="" type="checkbox"/>	shared_memory	clk	0x00002000	0x00002FFF		
<input checked="" type="checkbox"/>	sdram_0	clk	0x01000000	0x01FFFFFF		
<input checked="" type="checkbox"/>	epcs_controller	clk	0x00003000	0x000037FF	5	
<input checked="" type="checkbox"/>	tri_state_bridge_0	clk				
<input checked="" type="checkbox"/>	cfi_flash_0		0x00800000	0x00FFFFFF		
<input checked="" type="checkbox"/>	lan91c111_0		0x00010000	0x0001FFFF	6	0
<input checked="" type="checkbox"/>	spi_0	clk	0x00000820	0x0000083F	1	
<input checked="" type="checkbox"/>	uart_0	clk	0x00000840	0x0000085F	2	
<input checked="" type="checkbox"/>	pio_0	clk	0x00000860	0x0000086F		
<input checked="" type="checkbox"/>	pio_1	clk	0x00000870	0x0000087F		
<input checked="" type="checkbox"/>	timer_0	clk	0x00000880	0x0000088F	3	
<input checked="" type="checkbox"/>	timer_1	clk	0x000008A0	0x000008BF	4	

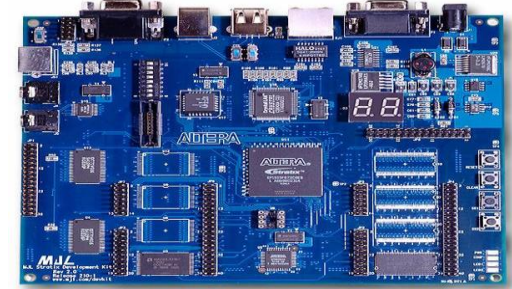
SOPC Builder

System RTL



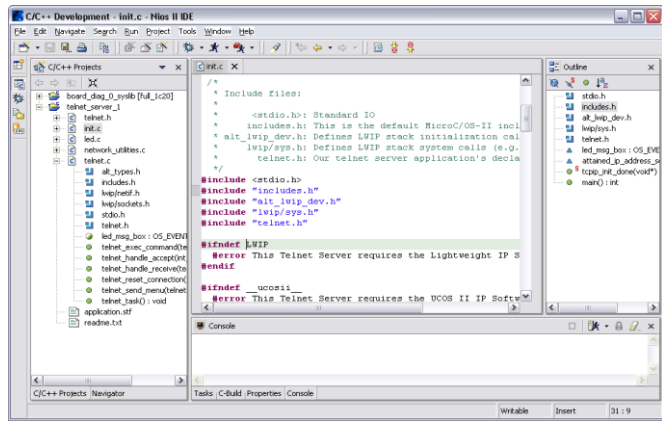
QUARTUS® II

Hardware Image



System Description File

Software Image



- Application creation
- Custom library

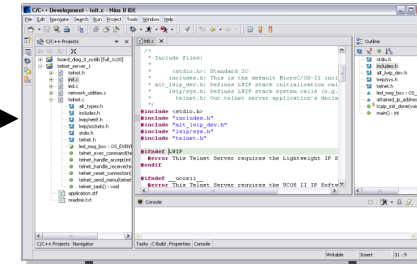
Nios II Integrated Development Environment (IDE)

Automatic Board Support Package (BSP) Generation

Use	Module Name	Clock	Base	End	IRQ	IRQ
✓	cpu_0	clk	0x00000000	0x000007FF	7	0
✓	cpu0_memory	clk	0x00001000	0x00001FFF	7	0
✓	dma_0	clk	0x00000800	0x0000081F	7	0
✓	cpu_1	clk	0x00000000	0x000007FF	7	0
✓	cpu1_memory	clk	0x00002000	0x00002FFF	7	0
✓	dma_1	clk	0x000008C0	0x000008DF	7	0
✓	shared_memory	clk	0x00002000	0x00002FFF	7	0
✓	sdram_0	clk	0x01000000	0x01FFFFFF	7	0
✓	epcs_controller	clk	0x00003000	0x000037FF	5	0
✓	tri_state_bridge_0	clk				
✓	cfi_flash_0		0x00800000	0x00FFFFFF	1	0
✓	lan91c111_0		0x00010000	0x0001FFFF	6	0
✓	spi_0	clk	0x00000820	0x0000083F	1	0
✓	uart_0	clk	0x00000840	0x0000085F	2	0
✓	pio_0	clk	0x00000860	0x0000086F	2	0
✓	pio_1	clk	0x00000870	0x0000087F	2	0
✓	timer_0	clk	0x00000880	0x0000089F	3	0
✓	timer_1	clk	0x000008A0	0x000008BF	4	0

System Description

Integrated Development Environment



Software Driver

Compiler

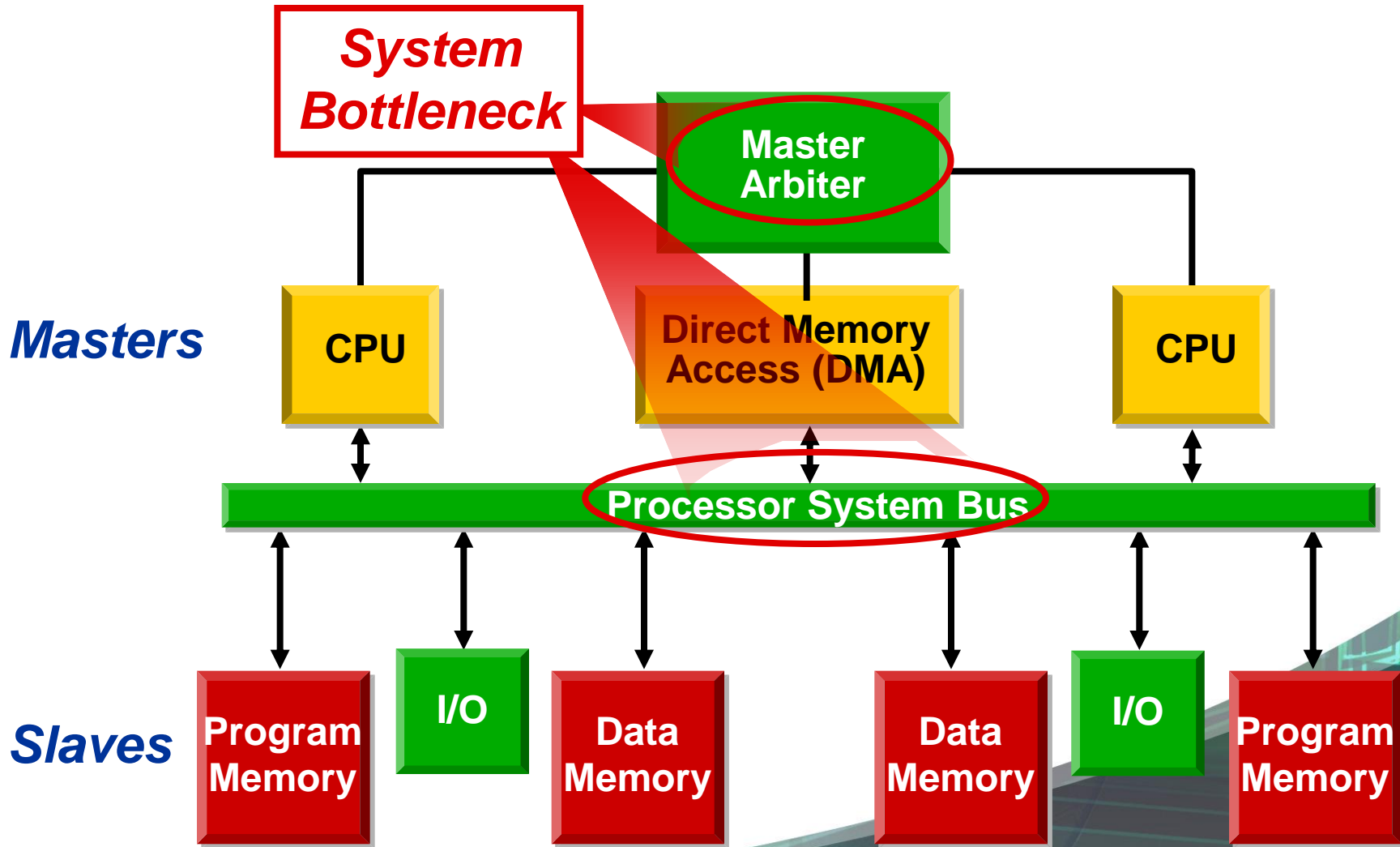
C Header

lib

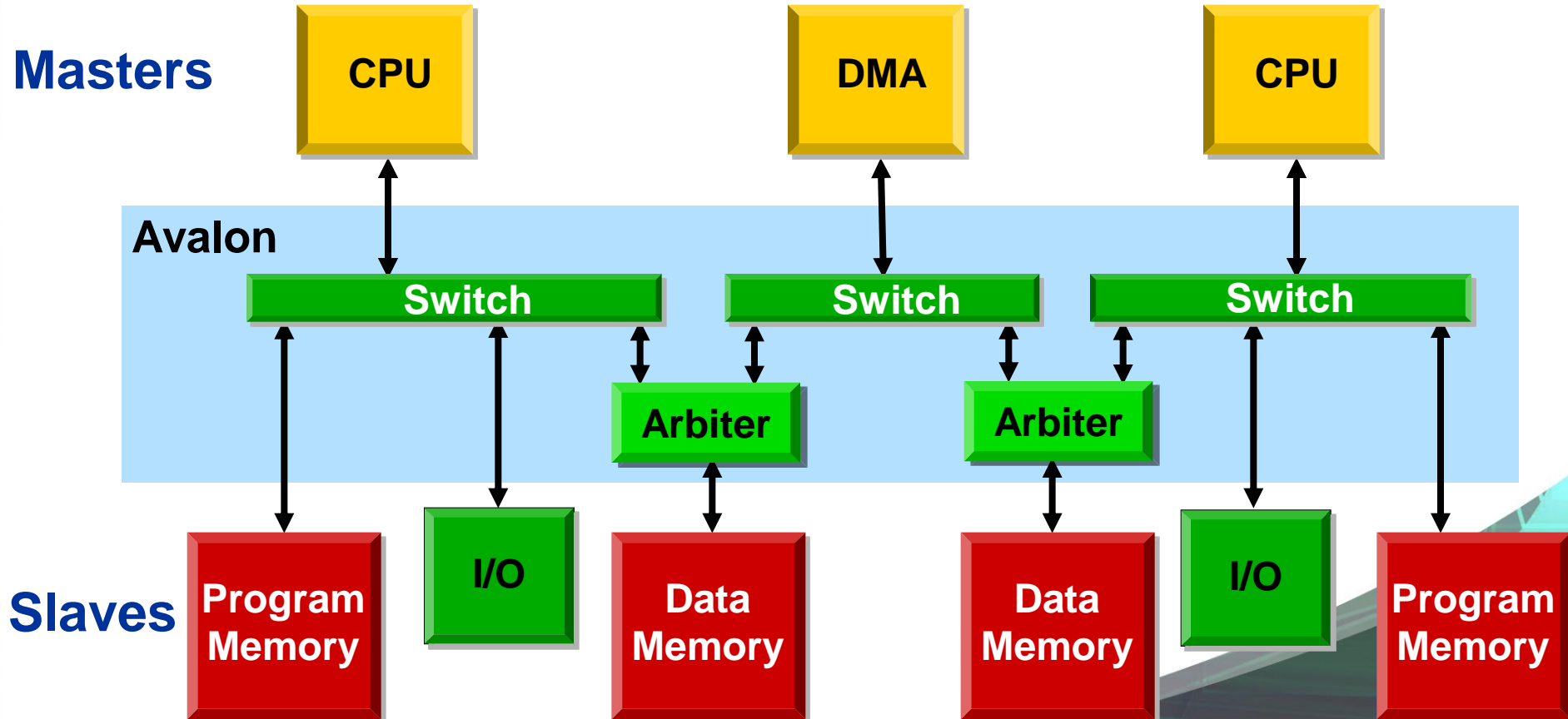
Avalon® System Interconnect

- Automatically generated for system
- Switches connect components – not a bus
- Slave side arbitration
 - Enables concurrent accesses
- Avalon functions
 - Arbitration
 - Multiplexing
 - Address decoding
 - Wait-state generation
 - Dynamic bus sizing

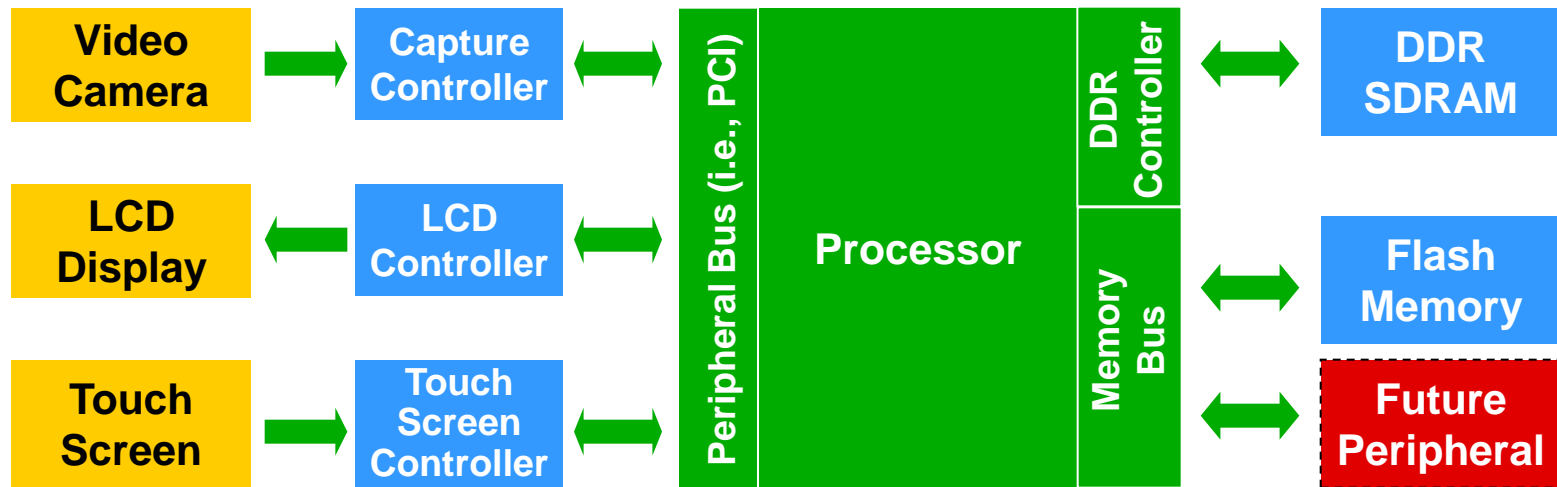
Traditional Bus Interconnect



System Interconnect



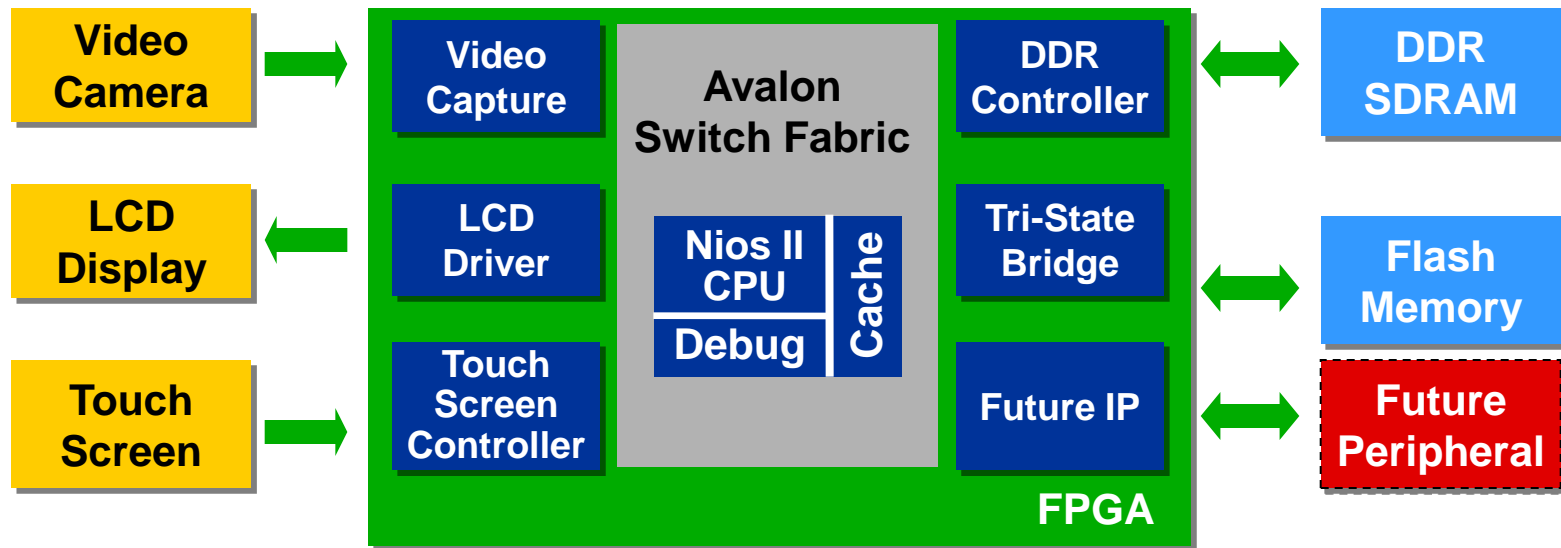
Video System Built “Conventionally”



■ Typical system construction steps

1. Specify external components and peripherals
2. Select processor with right...
 - Performance needed for application
 - Peripheral controller bus for controllers (i.e., PCI, PCIX, etc.)
 - Memory controllers

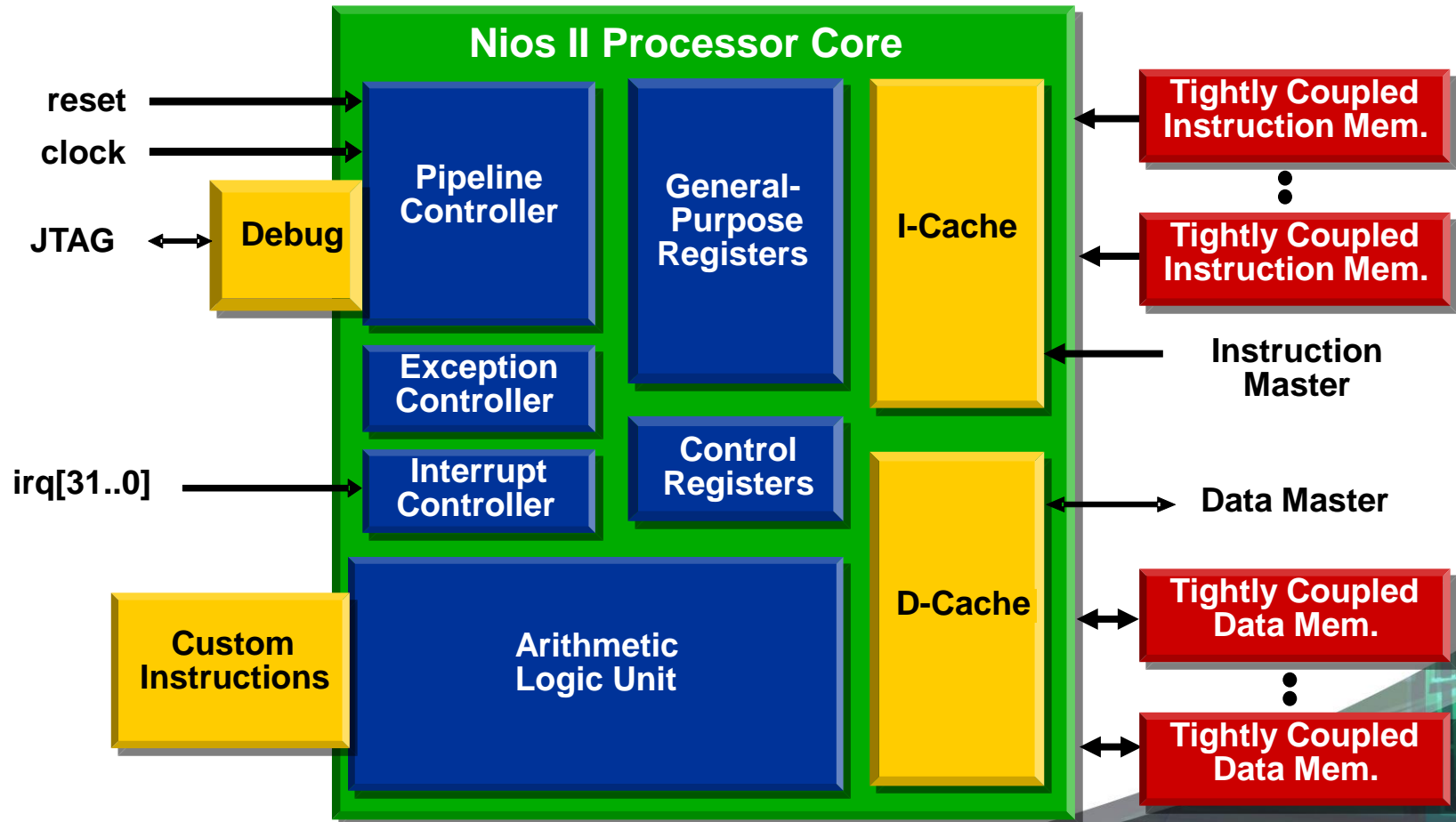
Video System Built With SOPC Builder



■ SOPC Builder-based construction

1. Specify external components and peripherals
2. Use SOPC Builder to:
 - Add peripherals and memory controllers
 - Add Nios II CPU
 - Configure system for maximum performance

Nios II Processor Block Diagram



Nios II: Classic RISC CPU

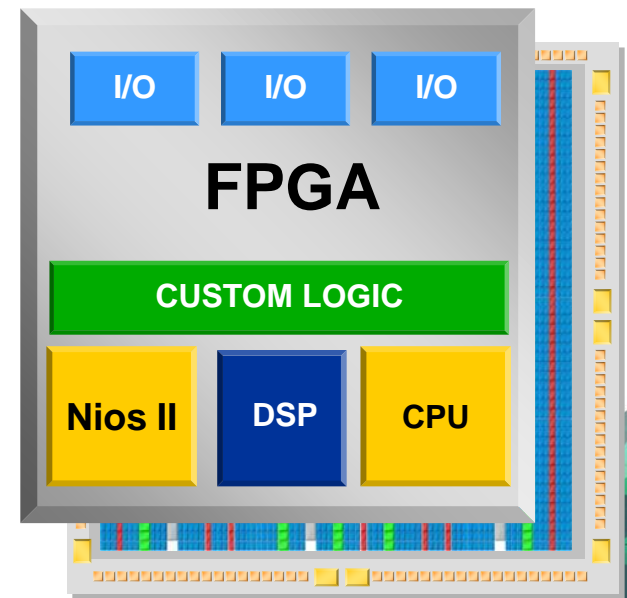
- Soft-core reconfigurable CPU
- Classic RISC architecture optimized for FPGA
 - 32-bit instruction set
 - 32-bit data path
 - 32 general-purpose registers
 - 3 instruction formats
 - 82 instructions
 - Instruction set is not configurable
 - Provides code compatibility for all implementations
 - Up to 256 custom instructions
 - 3 operand instructions (2 source, 1 destination)
 - Optional multiply and divide
- Strong performance
(up to 225 DMIPS)

NOW What We're Going to Do...

- Build a system with SOPC Builder
 - Add and parameterize peripherals
 - Nios II processor
 - Memory (DDR SDRAM)
 - Timer
 - JTAG UART
 - Pulse width modulator (custom peripheral)
 - Connect peripherals with Avalon switch fabric
 - Configure system for operation

Benefits of FPGA-Based Embedded Systems

- FPGA hardware, configurable processor and automated system generation deliver:
 - Fast development time
 - Reduced costs
 - Product differentiation
 - High performance
 - New features
 - Product life management
 - Protection against obsolescence
 - In-field upgrades



Thank You Q & A