Enhance System Performance and Productivity by Leveraging DSP and Embedded Technologies in FPGA Designs
Agenda

- Embedded and digital signal processing (DSP) design challenges and solutions
- DSP coprocessing
- Nios® II C-to-Hardware (C2H) Acceleration Compiler
- Quartus® II software highlighted features
- Conclusion
Product Evolution

1985
Mobile phone

2007
Phone, diary, email, SMS, web browser, alarm clock, calendar, voice recorder, radio, MP3 player, camera, etc...

Constant Demand for New Features; Higher Performance and Lower Costs
Embedded and DSP Design Challenges

**FPGAs Tackle These Challenges Head On**
Solution on Productivity—Tool

Hardware Design

- Design Idea
- Hardware Design Capture
  - RTL, Schematic
- RTL Synthesis
  - Nettlist
- “Fitting” (Map, Place, Route)
  - Post-Fit Nettlist
- Programming
  - Bitstream

System-Level Design

- Can My Engineers Construct Systems Quickly and Easily?
- Will My System Architecture Meet My Power Budget?
- Are The Power Estimates Reliable?
- Will the Software Automatically Optimize Power, and Still Meet Timing?
- Can My Software Engineers Accelerate Their Software Code?

Power Management

Software Design

- C, C++
- CPU Software Development
  - Object Code

Team Productivity

- Can Teams in Different Locations Work on the Same Project?
- Are We Using The Optimal System to Close Timing?
- Can My Engineers Reduce Their Compile Times?

Unique Quartus II Productivity Technologies

- Save Weeks to Months of Engineering Effort

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Solution on Flexibility—FPGAs

FPGA is the Poster Child for Flexibility; Rapidly Prototype System and Feature Fill Over Time
Solution on Performance (1): FPGA Single Chip
Solution on Performance (2): DSP+FPGA Coprocessing

Cool down
DSP Coprocessing
CPU Challenges

- Processor speedup isn’t there
- Performance limited by power
- Memory bandwidth limitations
- Single-core performance reaching a limit

Multi-core announcements by Intel, AMD, ARM, and others

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Processor Model Challenges For HPC

- Memory bandwidth limited by package and pin count
- Multiple caches required to keep the microprocessor busy
- Multi-processor cache coherency problem eats up performance gains
- Most of the power consumption is in the cache and related controllers
- But many HPC applications derive little or no benefit from cache

Source: Prof. John Wawrzynek, BWRC, UC Berkeley
Overall Customer Requirements

- **Performance**: 10X – 100X algorithm and 3X – 50X application acceleration
- **Productivity**: Simplicity of the tool chain; reduce the effort
- **Power**: Better performance-to-power ratio
- **Price**: Compared to alternatives
## Performance—FPGA Algorithm Acceleration

- **10X-100X at algorithm level**
- **Typically 3X-50X at application level**
- **Varies by vertical**
  - 10X for medical imaging
  - 20-50X for financial

<table>
<thead>
<tr>
<th>Application</th>
<th>Processor only</th>
<th>FPGA Processing</th>
<th>Speed Up</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hough and inverse Hough processing</td>
<td>12 minutes processing time Pentium 4-3 GHz</td>
<td>2 seconds of processing time @ 20 MHz</td>
<td>370x faster</td>
</tr>
<tr>
<td>AES 1MB data processing/crypto rate</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Encryption</td>
<td>5,558 ms/1.51 Mbps</td>
<td>424 ms/19.7 Mbps</td>
<td>13x faster</td>
</tr>
<tr>
<td>Decryption</td>
<td>5,562 ms/1.51 Mbps</td>
<td>424 ms/19.7 Mbps</td>
<td></td>
</tr>
<tr>
<td>Smith-Waterman search34 from FASTA</td>
<td>6461 sec processing time (Opteron)</td>
<td>100 sec FPGA processing</td>
<td>64x faster</td>
</tr>
<tr>
<td>Multi-dimensional hypercube search</td>
<td>119.5 sec (Opteron 2.2 GHz)</td>
<td>1.06 sec FPGA @ 140 MHz</td>
<td>113x faster</td>
</tr>
<tr>
<td>Callable Monte-Carlo analysis (64,000 paths)</td>
<td>100 sec processing time (Opteron 2.4 GHz)</td>
<td>10 sec of processing @ 200 MHz FPGA</td>
<td>10x faster</td>
</tr>
<tr>
<td>BJM financial analysis (5M paths)</td>
<td>6300 sec processing time (Pentium 4-1.5 GHz)</td>
<td>242 sec of processing @ 61 MHz FPGA</td>
<td>26x faster</td>
</tr>
<tr>
<td>Mersenne Twister random number generation</td>
<td>10M 32-bit integers/sec (Opteron-2.2 GHz)</td>
<td>319M 32-bit integers/sec</td>
<td>3x faster</td>
</tr>
</tbody>
</table>

Source: AMD
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Co-Processing Architectures

**Intel Xeon® Architecture**
- Uses Front Side Bus (FSB) Interconnect
- Latest North Bridge has FSB interface for each CPU

**AMD Opteron™ Architecture**
- Uses HyperTransport Interconnect
- Industry-standard AMD64 technology
- Socket modules available for Opteron
Commerciaically Available Platform

Innovation: build a simple, minimalist board with interfaces to HyperTransport and memory: (patent pending)

Drop-in replacement for an AMD Opteron with no changes to motherboard!

AMD Opteron Motherboard:

- Simply remove Opteron and replace with FPGA board!

X86 HPC Solution

Idea: build a simple, minimalist board with interfaces to HyperTransport and memory: (patent pending)

- Drop-in replacement for an AMD Opteron with no changes to motherboard!

FPGA uses all motherboard resources meant for CPU:
- HyperTransport links, memory interface, power supply, heat-sink

Usable with any AMD Opteron (or future Intel CSI-enabled CPUs) server

Usable in rack-mount or high-density, “blade” server systems, where
- Plug-in boards are not feasible

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C2H (C to Hardware) Tool
Boosting Software Performance

If you choose a faster processor

- More expensive $$$$$
- Consumes more power
- Requires board redesign
Boosting Software Performance

Multiply software performance. Accelerate only what’s necessary. Don’t pay for performance you don’t need.
Hardware Acceleration Flow

- Profile Code
- Identify Bottlenecks
- Re-partition Memory
- Identify Function to Accelerate
- Write HDL
- Software Driver
- Integration
- Benchmark
- Rebuild Project

Traditional Hardware Accelerator Design Flow

Time
Hardware Acceleration Flow

Nios II C-to-Hardware Acceleration Design Flow

Profile Code
Identify Bottlenecks
Re-partition Memory
Identify Function to Accelerate
Write HDL
Nios II C2H
Integration
Benchmark
Rebuild Project

Reduced Development Time

Time
Nios II C-to-Hardware Acceleration Compiler

- Productivity tool that automates creation and integration of hardware accelerators
- Streamlines C acceleration—you don’t have to know how to design hardware
- Integrated in familiar Eclipse-based Altera® Nios II Integrated Development Environment (IDE)

Right Click to Accelerate

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Step 1: Identify Software Bottlenecks

main ()
{ ...
  variable declarations...
  init();

  while (!error && got_data())
  {
    do_user_interface();
    gather_statistics();
    if (got_new_data())
      d_transform(in_buf, out_buf);
    check_for_errors();
  }
  cleanup();
}
main ()
{
    ...variable declarations...
    init();

    while (!error && got_data())
    {
        do_user_interface();
        gather_statistics();
        if (got_new_data())
        {
            d_transform(in_buf, out_buf);
            check_for_errors();
        }
    }
    cleanup();
}
What Does Nios II C2H Compiler Do?

- Generates a custom hardware accelerator from an ANSI C function

```c
13
14
15 int do_dma( int * __restrict__ dest_ptr,
16            int * __restrict__ source_ptr,
17            int length )
18 {
19  int i;
20
21  for( i = 0; i < (length / 4); i++ )
22   {
23     *dest_ptr++ = *source_ptr++;
24   }
25  return( 0 );
26}
```
Dramatic Performance Boost

- Auto Correlation: 1.4x
- Bit Allocation: 1.5x
- Convolution Encoder: 1.3x
- FFT: 2x

FFT: fast Fourier transform

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EEMBC Image Rotate

Software-implemented image rotate:
3773 iterations/second

Hardware-accelerated image rotate
3926 iterations/second

As fast as a 1.4-GHz processor for $1.42 of logic in a Cyclone® II FPGA

(95 MHz)
Quartus II Highlighted Features

• SOPC Builder
• PowerPlay
• TimeQuest
SOPC Builder – The Tool

- Automates block-based design
  - System definition
  - Component integration
  - System verification
  - Software generation

- Fast and easy

- Supports design reuse
  - 3\textsuperscript{rd} Party intellectual property (IP) Cores
  - Internally developed IP
SOPC Builder Tool at a Glance

- **Tabs**
- **List of Available Components**
- **Over 60 Cores available today**
- **Board settings**
- **Clock settings table**
- **IRQs defined**
- **Alterna, partner and user cores**
  - Processors
  - Memory interfaces
  - Peripherals
  - Bridges
  - Hardware accelerators
  - Custom peripherals

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SOPC Builder Generated System

Designer Only Needs to Worry About Peripheral Interface
Design Tool Flow

- Create FPGA project in Quartus II software
- Build embedded sub-system in SOPC Builder
- Integrate sub-system in Quartus II project
- Compile design to generate programming file
- Program FPGA on the board
- Create software and run on the processor on the FPGA
**Quartus II Software: PowerPlay**

Automatic power reduction for maximum productivity

Timing is always met, then power optimizations are implemented

Power-Optimized Design ✔
PowerPlay Power Analyzer

- Provides single interface for vectorless and simulation-based power estimation
- Uses improved power models
  - Based on HSPICE and silicon correlation
- Executing power analysis
  - Processing menu ⇒ Start ⇒ Start PowerPlay Power Analyzer
  - Scripting
Three Parts to Good Power Estimates

1. Accurate toggle rate data on each signal
2. Accurate power models of device circuitry
3. Knowledge of device operating conditions
PowerPlay Power Analyzer

Signal Activities

User Design (after Compilation) → PowerPlay Power Analyzer → Power Analysis Report

Operating Conditions
PowerPlay Power Inputs

- Signal activity file (.SAF)
  - ASCII text file generated by Quartus II software

- VCD
  - Generated by Quartus II software and 3rd-party simulators

- “Power Toggle Rate” and “Power Static Probability” assignments
  - Use Assignment Editor or Tcl file
  - Apply to specific entities/nodes

- Default toggle rate (12.5%)
  - Percentage of clock periods in which signal transitions
  - May also express as an absolute number of transitions per second
Other Input Data Used

- Operating conditions
- Clock timing assignments
  - Used to calculate internal signal activities
- Vectorless estimation
  - PowerPlay automatically derives signal activity for a node
  - Based on activity rates of signals feeding a node and functionality
  - Requires input signal activity data
- Capacitive loading
- Termination
- I/O standard
PowerPlay Power Analyzer Settings

- Enter single or multiple SAF/VCD files
  - Allows simulation of subdesigns separately
  - Enable glitch filtering to increase accuracy
    - Also recommend enabling glitch filtering during simulation
- Enter default toggle rates for inputs
- Enter toggle rate for rest of design
- Enable/disable vectorless estimation
**Faster TimeQuest Timing Analyzer**

- Improves productivity with faster timing closure
  - Improved compile times
  - Reduced memory usage
  - Improved timing constraint conversion from Altera’s classic timing analyzer to Synopsys design constraint (SDC)
TimeQuest Timing Analyzer

- Timing analysis
  - New, easy-to-use timing analyzer
  - Complete GUI environment for creating timing constraints and reports
  - Native support for SDC (Synopsis Design Constraints)

Only 65-nm FPGA Vendor with Native SDC Support
Top 5 Reasons to Use TimeQuest

- **Easier to use**: TimeQuest provides an easier to use GUI and interactive reporting for analyzing timing
- **Industry standard**: SDC format is an established industry standard
  - Simpler and more concise timing format
- **More powerful**: SDC allows for faster, easier description and analysis of advanced design constructs
  - DDR (other source sync.), complex clocks
- **Designs run faster**: TimeQuest more precisely analyzes timing behavior—gain 3-5% performance at 65 nm
- **Interoperability**: allows for easy migration of SDC constraints for ASIC and HardCopy® designs
Quartus II Reference

- Quartus II handbook
  - www.altera.com/literature/lit-qts.jsp

- Quartus II online demos
  - www.altera.com/quartusdemos

- Quartus II downloads
  - www.altera.com/download

- Technical support
  - www.altera.com/mysupport
Conclusion
FPGAs, Tools, and DSP–Coproprocessing Enhances Performance Together
Conclusion

- Embedded and DSP design challenges—productivity, performance, and flexibility
- DSP coprocessing, C2H tools, and new features in Quartus II help tackle those challenges
  - Coprocessing provides unparalleled performance improvement
  - C2H tools provide ability to create performance-enhancing hardware automatically (simply Right Click to Accelerate) without leaving the C domain
  - Quartus II SOPC Builder automates block-based design easily and efficiently; Powerplay automates power reduction for maximum productivity; Timequest facilitates timing analysis for 65-nm era and beyond
Thank You!