Designing with 6.375-Gbps Transceiver-Based FPGAs
Agenda

- Market trends in serial I/O protocols
- Transceiver-based FPGAs
- Designing with transceivers
- Protocol solutions
- Summary
Market Trends in Serial I/O
# Serial Interfaces

<table>
<thead>
<tr>
<th>Interconnect</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Long haul</td>
</tr>
<tr>
<td>Processor bus</td>
<td></td>
</tr>
<tr>
<td>Chip-to-chip</td>
<td></td>
</tr>
<tr>
<td>Backplane</td>
<td></td>
</tr>
<tr>
<td>Box-to-box</td>
<td></td>
</tr>
<tr>
<td>LAN</td>
<td></td>
</tr>
</tbody>
</table>

- **SerialLite II**
- **Serial RapidIO®**
- **XAUI**
- **CEI-6G**
- **PCI Express**
- **SD-SDI HD-SDI**
- **1G Ethernet**
- **SDH/SONET**

- Intra-system interconnect
- Inter-system interconnect

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Key drivers for Rel5/Rel6 were:

new data services
3GPP Long-Term Evolution Required to Enable Enhanced Services

3GPP evolution

New service creation

Service enhancement

Higher data rate

3G W-CDMA

Interactive gaming

Bi-directional HDTV

High-speed downloading

3D visualization

Integrated multimedia

As wired services

Text-based Internet services (BBS, Gopher, Usenet)

Text-oriented Web services

Basic multimedia Web services (audio, video streaming) interactive network gaming

Peer-to-peer services (Napster) Fast uploading services

VoD with HD quality Home networking

Modem (2.4 Kbps~56 Kbps)

ISDN (128 Kbps)

ADSL (1.5 Mbps~6 Mbps)

VDSL (10 Mbps~30 Mbps)

FTTH (~50Gbps)
Broadcast Market Trends – High Definition

- HD perhaps as big a change as black-and-white to color transition
- Studio dilemma: Both 1080i and 720p used for broadcast, so they need to store in 1080p (or higher) to preserve quality

3G-SDI and 10 GbE in the studio and headend in not too distant future
  - Beyond 3G-SDI, feasibility of 10 Gbps over coax already demonstrated
IPTV Distribution

Multicast Requirements for Video Driving Ethernet Aggregation Market

Source: Metro Ethernet Forum
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Serial Interfaces Benefits

- Transition from parallel to serial I/O solutions will:
  - Reduce system costs and simplify system design
  - Provide scalability to meet new bandwidth requirements
  - Drive broadbase adoption of serial standards, e.g. PCI Express, Serial RapidIO, Gigabit Ethernet

- High-speed serial I/O solutions will ultimately be deployed in nearly every type of electronic product imaginable!
Transceiver-Based FPGAs
Transceiver-Based FPGAs

FPGA vendors have introduced transceiver-based FPGAs
- Altera has 4 generations of transceiver products: Mercury™ programmable ASSPs, and Stratix® GX, Stratix II GX, and Arria™ GX FPGAs

Benefits
- Integration of transceivers with FPGAs increases bandwidth and reduces pin-count requirements
- Lower system cost
- Support for standard protocols as well proprietary protocols
- Respond to market dynamics with feature upgrades
Stratix II GX and Arria GX FPGAs Market Play

Flexible devices for high-performance, high-density logic and a wealth of protocol solutions

Protocol-targeted devices with a cost structure similar to ASSPs and with the flexibility of the FPGA fabric

Devices for specific protocols. As chip development costs rise, there are fewer ASSPs available
Protocol Solutions from 0.6 to 6.375 Gbps

- Addressable by Stratix II GX FPGAs
- Achievable by Stratix II GX FPGAs with oversampling
- Mainstream protocols supported by Arria GX FPGAs

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“Typical” Arria GX Bridging Application

- PCI Express devices
  - Freescale PowerQUICC III
  - Freescale e500-based microcontroller units (MCUs)
  - Freescale StarCore digital signal processing (DSP) devices
  - Southbridges (Intel, VIA, …)
  - Switches (IDT, PLX, …)
  - Graphics and networking chips

- GbE devices
  - Any device with GbE or triple-speed Ethernet support

- Serial RapidIO devices
  - TI TMS320C645x DSPs
  - Freescale StarCore-based DSPs
  - Freescale PowerQUICC III
  - Switches (Tundra, IDT, …)
Arria GX FPGA-Based Embedded Controller

- Altera Nios® II embedded controller
- Peripherals and interfaces
  - Memory controller
  - Gigabit Ethernet, PCIe, ...
  - Legacy PCI
  - Proprietary protocols
Stratix II GX FPGAs: Highlights

- Triple-speed Ethernet, 10 GbE/XAUI, Serial RapidIO standard, SD/HD/3G-SDI, SerialLite II
- FibreChannel @ 1,2 and 4 Gbps
- Sonet/SDH line jitter compliance for OC-3, OC-12, and OC-48
- PCI Express 1.0, 1.1 compliant and 2.0 ready @ 5 Gbps
- Interlaken support @ 6.375 Gbps and CEI-6 jitter compliance
- Adaptive equalization and hot-socketing for Plug and Play Signal Integrity
- Dynamic reconfiguration for “one-hardware-fits-all” applications

Fully Characterized Transceivers With Optimal Signal Integrity
Transceiver Block Hardware Support

- Two clock domains and two transmit phase locked loops (PLLs) in each transceiver block
- Different data rates by local clock dividers in each transmit channel
- Configuration port from programmable logic device (PLD) for on-the-fly reconfiguration
Dynamic Reconfiguration Scope

- Change transmit and receive PMA settings
  - Output differential voltage $V_{od}$
  - Transmitter pre-emphasis
  - Receiver equalization

- Change data rates for one protocol

- Change channel operational mode (>30 modes available)

- Allows a “one-hardware-fits-all” approach

- Eliminates system downtime
  - In-system upgrades
  - In-system signal integrity optimization, e.g. for backplanes
  - Hardware integration, test, and debug
Dynamic Reconfiguration Implementation

- New transceiver channel configuration without reconfiguring the FPGA
- Hitless for adjacent channels
- New channel configuration stored in memory
Best-in-Class Signal Integrity

Simulated Receive Eye, with No Equalizer

Simulated Receive Eye, with 17dB Equalizer

Eye Opening After 40” Backplane

Eye Opening After 40” Backplane and 9.5dB Pre-emphasis

Receive 6.375 Gbps

Transmit 6.375 Gbps
System Backplane Requirements

- Transceivers can easily drive 50-inch trace at 6.375 Gbps on FR-4 PCB material
- Pre-emphasis and equalization capabilities
- Specific set of pre-emphasis and equalization values dependent on the slot position
- Changing operating conditions and aging
- Ability for hot-swapping of cards
Adaptive Dispersion Compensation Engine (ADCE)

- Automatically monitors and adjusts the receive equalizer for the best eye opening
- Typical systems don’t require pre-emphasis for low bit error ratio (BER)
- Combined with pre-emphasis, the ADCE’s adaptive equalization results in very low BER
- On-chip hot-socketing transceiver support

Plug and Play Signal Integrity with Adaptive Equalization and Hot Socketing
Designing with Transceivers
Success Factors for Transceiver-Based Designs

Designing With Transceivers is Not About Silicon Alone
Optimal Signal Integrity

- Stratix II GX FPGA can drive 50” of backplane at 6.375 Gbps
- Comfortable margin for designers
- Lowest jitter and compliance to all standards
- Plug and play with ADCE, pre-emphasis, and equalization
Transceiver MegaWizard

Simplifies Transceiver Design
Altera’s PELE (Pre-emphasis and Equalization Link Estimator)

Proprietary EDA tool for determining pre-emphasis and equalization coefficients
Online Access to Eye Diagrams

- View thousands of eye diagrams
  - Enter channel parameters
Complete Protocol Solutions

- Hard protocol intellectual property (IP), IP core functions, reference designs
- Signal integrity modeling
- Protocol-specific development boards
  - PCI Express and SDI
- Evaluation board
- Quartus® II design software support
- Compliance testing
- System validation reports
- Characterization reports

Dramatically Increase Ease of Design
Large network of high-speed experts to support system-level integration

- Regional Support Centers (RSCs) in North America, Europe, Asia, and Japan
- Field-based high-speed specialist Field Applications Engineers (FAEs)
- Knowledgeable regional FAEs proficient in transceiver technology
- Online support (MySupport)
- Extensive collection of collateral, design examples, and characterization reports
Altera-TSMC Symbiotic Partnership

**Benefit to Altera:**

<table>
<thead>
<tr>
<th>What Altera gets:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Access to most advanced process without huge R&amp;D investments</td>
</tr>
<tr>
<td>Pure play foundry—no capacity conflict</td>
</tr>
<tr>
<td>Mutual benefit of an exclusive relationship</td>
</tr>
<tr>
<td>Ability to get process tuned to its needs</td>
</tr>
</tbody>
</table>

**Benefit to TSMC:**

<table>
<thead>
<tr>
<th>FPGA structure</th>
<th>What TSMC gets:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory structure</td>
<td>Defect identification</td>
</tr>
<tr>
<td>Large dies</td>
<td>Defect density (DD) reduction</td>
</tr>
<tr>
<td>Dense interconnect</td>
<td>Back-end improvements</td>
</tr>
<tr>
<td>High performance</td>
<td>Front-end improvements</td>
</tr>
</tbody>
</table>
PCI Express Solution

- Complete, easy-to-use PCI Express solutions
  - x1, x4 and x8 endpoints
  - Industry-leading design flow with Altera IP MegaCore®
  - Stratix II GX, Cyclone II, Stratix II, HardCopy II and Stratix GX device family support

- Low-risk, hardware-verified solutions
  - Device characterization and PCI-SIG compliance workshops
  - 2 generations of FPGAs with embedded transceivers
    - Stratix GX FPGA passed PCI-SIG compliance
    - Stratix II GX FPGA passed PCI-SIG compliance
  - Development/demo boards

Fastest Time-To-Market with a Reliable PCI Express Endpoint Solution
Availability – IP Core

- **PCI Express 1.1 compliance**
- Support for up to 4 virtual channels (VCs)
- Configurable maximum payload up to 2 Kbytes
  - 128, 256, 512, 1024, or 2048 Bytes
- Configurable retry buffer
- Optional end-to-end cyclic redundancy code (ECRC) generation/checking
- Optional advanced error reporting (AER)
- Flexible reference clock support (100, 125, or 156.25 MHz)
## PCI-SIG Compliance and Interoperability

### Test equipment vendor

<table>
<thead>
<tr>
<th>Test equipment vendor</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wavecrest</td>
<td>Passed</td>
</tr>
<tr>
<td>Agilent</td>
<td>Passed</td>
</tr>
<tr>
<td>Catalyst</td>
<td>Passed</td>
</tr>
<tr>
<td>Tektronix</td>
<td>Passed</td>
</tr>
<tr>
<td>VMETRO</td>
<td>Passed</td>
</tr>
<tr>
<td>Intel</td>
<td>Passed</td>
</tr>
<tr>
<td>LeCroy</td>
<td>Passed</td>
</tr>
</tbody>
</table>

### Motherboard vendor

<table>
<thead>
<tr>
<th>Motherboard vendor</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel</td>
<td>Passed</td>
</tr>
<tr>
<td>HP</td>
<td>Passed</td>
</tr>
<tr>
<td>IBM</td>
<td>Passed</td>
</tr>
<tr>
<td>ATI</td>
<td>Passed</td>
</tr>
<tr>
<td>NVIDIA</td>
<td>Passed</td>
</tr>
<tr>
<td>VIA</td>
<td>Passed</td>
</tr>
</tbody>
</table>

### Bridge/switch tested

<table>
<thead>
<tr>
<th>Bridge/switch tested</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLX</td>
<td>Passed</td>
</tr>
<tr>
<td>IDT</td>
<td>Passed</td>
</tr>
</tbody>
</table>

### Interoperability

<table>
<thead>
<tr>
<th>Interoperability</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Freescale PowerQUICC III</td>
<td>Passed</td>
</tr>
<tr>
<td>IDT Switches</td>
<td>Passed</td>
</tr>
</tbody>
</table>

*Passed all the PCI-SIG Gold-Suite Compliance Tests with 100% Pass Rate*
Gigabit Ethernet Solution

- Single device solution
- Lowest power per lane
- IEEE 802.3-compliant PCS and PMA
  - Chip-to-chip
  - Board-to-board
  - Backplane
  - SFP fiber optics
- Flexibility
  - Implement the GbE ports required by your unique application
    - 1, 2, 3, … 20 ports
Triple Speed Ethernet (TSE) MegaCore

- Single to multiple port 10-/100-Mbps or 1-Gbps Ethernet applications
- LAN and WAN data plane or control plane (embedded system) applications
- Chip-to-chip, board-to-board, and inter-system network connectivity

FPGA

MAC
- TX FIFO
- TX Control
- RX FIFO
- RX Control
- STATS
- HOST INT’FC
- MGM’T

PCS
- Frame Encapsulation
- Auto Negotiation
- De-Encapsulation
- Synchronization
- 8b/10b Encoder
- 8b/10b Decoder

PMA
- Serializer
- CDR & De-Serializer

Optional External Copper or Optical PHY (PMD)

External Network

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MorethanIP Ethernet Solutions Spectrum

TCP-IP Acceleration

10 Gigabit Ethernet

Storage

Site A

12.5 HiGig+ / HiGig2

Site B

2.5 Gigabit Ethernet

Extranet (Suppliers)

Ethernet Switching

10/100 Ethernet

POP
P2P (Metro)

10/100/1000 Ethernet

10/100/1000 Ethernet

EFM / EPON

www.moretthanip.com
Altera Stratix II GX RapidIO Solution

- RapidIO MegaCore® Version 6.1
- Compliant with RapidIO Trade Association, RapidIO Interconnect Specification, Revision 1.3
- Physical layer features
  - 1x/4x serial
    - Stratix II GX support, including 1x and 4x up to 3.125 Gbps
  - 8-bit parallel
- Transport layer features
  - Supports multiple logical layer modules
  - Supports 8-bit device identities (IDs)
- Logic layer features
  - Maintenance master and slave logical layer module
  - I/O master and slave logical layer module
  - Doorbell support
- PCI Express development kit expansion via HSMC connectors to AMC module
- SRIO loopback example design available based on the Signal Integrity kit
- Other IP vendors: Mercury Computers, GDA Technologies, Jennic, Preasum
SDI in Broadcast Studio Application

Capture
Switching
Editing
Special Effects
Mixing
Compression
Storage
Encoding
Monitoring

Video Switcher
(Master Control,
Production)

Off-Line Editing:
VTR, VDR, NLE,
Char. Gen.,
Archive and Rest.,
and more

Video Router

CODEC

Video Servers

SD/HD-SDI

Other

Studio, Head-End Transmission Network

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SDI MegaCore

- SD-, HD-, and 3G-SDI support in version 6.1
- Multi-rate SD/HD-SDI support
- Full duplex implementation – transmit and receive channel
- Transmit features
  - CRC encode
  - Line number insertion
- Receive features
  - CRC decode
  - Line-number extraction
  - Framing and extraction of video timing signals
  - Receiver format detector
- SD transmit word scrambler
- SD receive word alignment and descrambler
- SMPTE-compliant SD and HD interfaces
SONET/SDH Overview

- Stratix II GX FPGA telecom protocol support

<table>
<thead>
<tr>
<th>SONET signals</th>
<th>SDH signals</th>
<th>Line rate (Mbps)</th>
<th>Stratix II GX FPGAs</th>
</tr>
</thead>
<tbody>
<tr>
<td>STS-3</td>
<td>OC-3</td>
<td>STM-1</td>
<td>155.52</td>
</tr>
<tr>
<td>STS-12</td>
<td>OC-12</td>
<td>STM-4</td>
<td>622.08</td>
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<tr>
<td>STS-48</td>
<td>OC-48</td>
<td>STM-16</td>
<td>2,488.32</td>
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<tr>
<td>STS-96</td>
<td>OC-96</td>
<td>STM-32</td>
<td>5,576.64</td>
</tr>
<tr>
<td>STS-192</td>
<td>OC-192</td>
<td>STM-64</td>
<td>9,953.28</td>
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<tr>
<td>STS-768</td>
<td>OC-768</td>
<td>STM-256</td>
<td>39,813.12</td>
</tr>
</tbody>
</table>

- Line side applications
  - Stringent jitter requirements

- Backplane applications
  - Less reliant on jitter specifications

Stratix II GX Devices Support Backplane and Line Side Applications
Hard Protocol IP in Stratix II GX Transceiver

- **PMA support**
  - SDH/SONET jitter line side compliant for
    - STM-4/OC-12 and STM-16/OC-48
  - Dynamic reconfiguration enables multi-rate support

- **PCS support**
  - MSB serializer/deserializer (SERDES) support
  - Word alignment support A1,A2 and A1,A1, A2,A2 frame characters
  - Byte re-ordering (OC-48/STM-16)
  - Support for 8/16/32 data path
SONET/SDH Characterization

- Stratix II GX devices are the only SONET/SDH-compliant FPGAs in the industry!
- SONET/SDH backplane and line side compliant over PVT with margin!
  - Jitter tolerance = receive jitter
  - Jitter generation = transmit jitter
  - Run length
- Characterization completed for OC-3/STM-1 (oversampling), OC-12/STM-4, and OC-48/STM-16 line rates
  - Margin provided to allow for optical modules
  - SONET/SDH OC-3, OC-12, and OC-48 characterization report available
Stratix II GX SerialLite II Solution

- Altera’s second-generation lightweight serial interconnect protocol
- Point-to-point
  - Chip-to-chip, board-to-board, backplane
- Physical and data link layers only
- Quick link-up time, low latency, light on logic
- Easy to implement
Market Segments and Applications

SLite2

Sensor

SFP
SFP

SLite2

Sensor

SFP
SFP

SLite2

Sensor

SFP
SFP

SLite2

SLite2

SLite2

Memory

x8 PCI Express

x8 PCIe

Broadcast - Receives streaming data, transmits status and control

Simplex Tx - Transmits streaming data

Simplex Rx - Receives status and control
## Standards Compliance Check List

<table>
<thead>
<tr>
<th>Standard</th>
<th>Compliant</th>
<th>Documentation</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEI 6G SR/LR</td>
<td>Yes</td>
<td>Characterization Report</td>
</tr>
<tr>
<td>CPRI</td>
<td>Yes</td>
<td>Meets latency requirements</td>
</tr>
<tr>
<td>1/2/4G Fibre Channel</td>
<td>Yes</td>
<td>Characterization Report</td>
</tr>
<tr>
<td>GbE</td>
<td>Yes</td>
<td>Characterization Report</td>
</tr>
<tr>
<td>GPON</td>
<td>Yes</td>
<td>Characterization Report</td>
</tr>
<tr>
<td>HiGig+</td>
<td>Yes</td>
<td>Characterization Report</td>
</tr>
<tr>
<td>Interlaken</td>
<td>Yes</td>
<td>Characterization Report (CEI)</td>
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<tr>
<td>PCIe</td>
<td>Yes</td>
<td>Characterization Report</td>
</tr>
<tr>
<td>SD/HD/3G SDI</td>
<td>Yes</td>
<td>Characterization Report</td>
</tr>
<tr>
<td>SFI-5</td>
<td>TBD</td>
<td>Meets transmit skew</td>
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<tr>
<td>SONET OC-48</td>
<td>Yes</td>
<td>Characterization Report</td>
</tr>
<tr>
<td>SONET OC-3/12</td>
<td>Yes</td>
<td>Characterization Report</td>
</tr>
<tr>
<td>1.25/2.5/3.125 SRIO</td>
<td>Yes</td>
<td>Characterization Report</td>
</tr>
<tr>
<td>XAUI</td>
<td>Yes</td>
<td>Characterization Report</td>
</tr>
</tbody>
</table>
Summary

- Altera meets market trends for serial I/O protocols
- Stratix II GX and Arria GX FPGAs offer best-in-class transceivers with optimal signal integrity
  - Dynamic reconfiguration
  - ADCE, pre-emphasis, equalization
  - Support tools and IP
- Support for wide range of applications and protocols
Thank You!