Optimizing Performance using 65-nm Architecture
## Agenda

- Evolution of FPGAs and customer challenges
- Stratix® III architecture designed for high performance
- Performance benchmarks for Stratix III FPGAs
- Power optimization in Stratix III FPGAs
- Summary
Evolution of FPGAs—Usage and Customer Challenges
Evolution of FPGA Usage

Today’s FPGAs Have Evolved
Issues and Challenges in FPGA Projects for Asia

EETimes - 2006 EDA Times Study

<table>
<thead>
<tr>
<th>Issue</th>
<th>2006</th>
<th>2007</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>Completing functional verification</td>
<td>53%</td>
<td>51%</td>
<td>-2%</td>
</tr>
<tr>
<td>Meeting timing budgets</td>
<td>51%</td>
<td>34%</td>
<td>-17%</td>
</tr>
<tr>
<td>Getting it to work on the PCB</td>
<td>41%</td>
<td>25%</td>
<td>-16%</td>
</tr>
<tr>
<td>Managing complexity</td>
<td>37%</td>
<td>36%</td>
<td>1%</td>
</tr>
<tr>
<td>Lengthy design cycles</td>
<td>34%</td>
<td>26%</td>
<td>-8%</td>
</tr>
<tr>
<td>Engineering productivity</td>
<td>34%</td>
<td>20%</td>
<td>-14%</td>
</tr>
<tr>
<td>Design for test</td>
<td>33%</td>
<td>20%</td>
<td>-13%</td>
</tr>
<tr>
<td>Signal integrity</td>
<td>28%</td>
<td>24%</td>
<td>-4%</td>
</tr>
<tr>
<td>Pin assignment closure</td>
<td>27%</td>
<td>15%</td>
<td>-12%</td>
</tr>
<tr>
<td>Meeting cost budgets</td>
<td>23%</td>
<td>22%</td>
<td>1%</td>
</tr>
<tr>
<td>Tool interoperability</td>
<td>21%</td>
<td>16%</td>
<td>-5%</td>
</tr>
<tr>
<td>IP selection/verification</td>
<td>21%</td>
<td>10%</td>
<td>-11%</td>
</tr>
<tr>
<td>Meeting power budgets (active/dynamic)</td>
<td>23%</td>
<td>20%</td>
<td>-3%</td>
</tr>
<tr>
<td>Minimizing die size</td>
<td>18%</td>
<td>15%</td>
<td>-3%</td>
</tr>
<tr>
<td>Meeting power budgets (leakage)</td>
<td>18%</td>
<td>15%</td>
<td>-3%</td>
</tr>
</tbody>
</table>

* 'Very critical' - at current process geometry
* 'Getting worse' - as process geometries shrink
* *Added in 2006

Performance, Productivity, Power, and Price

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Stratix III FPGAs Address FPGA Design Challenges

- **Performance**
  - Industry’s highest performance FPGA

- **Power**
  - Industry’s lowest power high-end FPGA with innovative Programmable Power Technology
  - Net Seminar: Learn to Design with Stratix III FPGA’s Programmable Power Technology and Selectable Core Voltage (April 2007)

- **Productivity**
  - Quartus® II software: #1 in performance and productivity
  - Net Seminar: How to Maximize Performance and Productivity for Stratix III Using Quartus II Software (June 2007)

- **Price**
  - Patented redundancy reduces cost automatically
  - Risk-free path to structured ASIC – HardCopy® devices
  - Please visit [www.altera.com](http://www.altera.com) for more details
Benefits of Higher Performance

- Allows faster time-to-market
  - Reduces effort for timing closure
- Provides extra operating margins for extreme conditions
- Saves cost
  - Achieves performance goals with lower speed grade devices
  - Serializes parallel logic to use lower density device
- Allows path for future system upgrades
- Provides extra horsepower if your design needs it
Achieving Performance using Stratix III Devices
Stratix III FPGAs Built with Performance in Mind

- Advanced 65-nm process
- High-performance architecture
- Integrated tools solution with Quartus II software
Stratix III FPGAs Built on Leading-Edge Process Technology

- Advanced 65-nm process
  - 15% capacitance reduction → reduces dynamic power and increases performance
- Strained silicon
  - Increased performance
- Low-k inter-metal dielectric
  - Reduces dynamic power, increases performance
- Copper interconnect
  - Increased performance, reduced IR drop
- Multiple-gate oxide thicknesses (triple oxide)
  - Trade-off of power vs. speed per transistor
- Multiple-threshold voltages
  - Trade-off of power vs. speed per transistor

Stratix III FPGAs Built for Increased Performance and Reduced Power
Innovative Adaptive Logic Module

Innovative adaptive logic module (ALM) introduced in 2004

Stratix III FPGAs Built On a Highly Flexible ALM Architecture
One Look-up Table (LUT) Size Does Not Fit All

* Results on real customer benchmarks

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ALM Adder Tree Support

Stratix III ALM 3-Input Adder Tree

2-Input Adder Tree

16-Bit 128-Input Adder

Less Logic Required – Increased Performance

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Stratix III DSP Block Summary

[Diagram showing the Stratix III DSP block with input register unit, optional pipelining, output multiplexer, optional RND & SAT unit, and output register unit.]

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Performance Through Parallelism

EP3SL150

Total 18x18 multipliers = 384
Max clock freq = 550 MHz
Max performance = 384 * 550 MHz

211 GMACS
DSP Advantages of Stratix III FPGAs

Stratix III FPGAs deliver 50X performance over dedicated digital signal processing (DSP) devices
- Parallel processing
- High memory- and multiplier-to-logic ratios
Stratix FPGAs for High-Performance DSP

**Stratix III EP3SL70**
- 300 MHz
- 86 GMACS
- ~3 Watts
- ~1,225 mm²
- ~$400 in 1KU

*Note: Stratix III EP3SL70 FPGA is small logic-oriented device*

For Equivalent Performance, Stratix III FPGAs Provide
Lower Cost, Low Power, and Reduced Board Space

DSP @ 1 GHz
- 80 GMACS
- ~10-15 Watts
- ~5,000 mm²
- ~$300/per DSP device in 1KU
- ~$3,000 total
Clock Networks and PLLs

Abundant clock resources
- Easy placement and routing utilizing a 600-MHz clock network
- Up to 88 regional clock networks for fewer fanouts and fast local clock

All clock networks automatically powered down when not in use

High-performance and flexible phase locked loops (PLLs)
- Up to 12 PLLs per device, each with up to 10 outputs per PLL
- 5- to 720-MHz output with inherent jitter filtration

High-Performance Clocking Scheme at 600 MHz
Software-Driven Architecture

- Architecture-optimized software tool implementation critical to achieve
  - Increased performance and reduced power
  - Efficient logic utilization
  - Enhanced productivity

FPGA Architecture Only as Good as the Software Can Exploit
Altera’s FPGA modeling tool (FMT)
- Enables Altera to virtually model a variety of FPGA structures to achieve an optimal, well integrated architecture
- FMT provides in-depth modeling capabilities and their effects on performance, area, and cost
Quartus II Key Features

- Design space explorer
  - Automated utility to find settings for the best performance

- Incremental compile
  - Optimizes performance by block and maintains the overall performance

- TimeQuest timing analyzer
  - Supports Synopsys Design Constraint (SDC), an industry-standard tool, for faster analysis of advanced design constructs

- PowerPlay optimization
  - Localizes high-toggling nets, and routes for minimum capacitance to maximize your performance while lowering power

Quartus II Software is Stratix III FPGA--Ready

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Performance Comparison of Stratix III and Stratix II FPGAs
Stratix III FPGAs: Highest Performance

Stratix III advantage

Stratix II advantage

Low Power Without Sacrificing Performance

Stratix III FPGAs are 35% Faster than Stratix II FPGAs
## Stratix III FPGA Performance Scorecard

<table>
<thead>
<tr>
<th>Block</th>
<th>Stratix II Devices</th>
<th>Stratix III Devices **</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Fabric</td>
<td>500 MHz</td>
<td>600 MHz</td>
</tr>
<tr>
<td>Small RAM</td>
<td>500 MHz</td>
<td>600 MHz</td>
</tr>
<tr>
<td>Medium RAM</td>
<td>550 MHz</td>
<td>600 MHz</td>
</tr>
<tr>
<td>Large RAM</td>
<td>400 MHz</td>
<td>600 MHz</td>
</tr>
<tr>
<td>DSP Block</td>
<td>450 MHz</td>
<td>550 MHz</td>
</tr>
</tbody>
</table>

** Pending characterization
Stratix III FPGA I/O Connectivity

- High flexibility and efficiency
  - Modular bank structure
  - Supports over 40 industry I/O standards with adjustable slew rate, drive strength, and output delay
  - Dynamic trace compensation for trace mismatch per I/O

- Enhanced on-chip termination (OCT)
  - Dynamic OCT changes termination dynamically
  - Calibration gives repeatable and predictable termination

High-Performance I/Os
I/O Performance

- LVDS and external memory interfaces support on all I/O banks

<table>
<thead>
<tr>
<th>Interconnect</th>
<th>Stratix II FPGA Definition</th>
<th>Stratix III FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR3</td>
<td>N/A</td>
<td>400 MHz</td>
</tr>
<tr>
<td>New</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DDR2</td>
<td>333 MHz</td>
<td>400 MHz</td>
</tr>
<tr>
<td>QDR II</td>
<td>300 MHz</td>
<td>350 MHz</td>
</tr>
<tr>
<td>QDR II+</td>
<td>N/A</td>
<td>350 MHz</td>
</tr>
<tr>
<td>New</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RLDRAM II</td>
<td>300 MHz</td>
<td>400 MHz</td>
</tr>
<tr>
<td>New</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LVDS</td>
<td>1.0 Gbps</td>
<td>1.25 Gbps</td>
</tr>
<tr>
<td>Dynamic Phase Alignment (DPA)</td>
<td></td>
<td>Dynamic Phase Alignment (DPA)</td>
</tr>
<tr>
<td>PCI, PCI-X</td>
<td>3.3-V Compliant</td>
<td>3.3-V Compatible</td>
</tr>
</tbody>
</table>

* Stratix III FPGA left and right banks support 300-MHz DDR.
Stratix III FPGA top and bottom banks support 800-Mbps LVDS input and 500-Mbps output using a 3-resistor network.

**Pending characterization**
Architecture Comparison of Stratix III and Virtex-5 FPGAs
Stratix III ALM vs. Virtex-5 LUT-FF Pair

Stratix III ALM—Flexible, Efficient, and Industry’s Best FPGA Logic Architecture
Stratix II ALM 8-Input Fracturable Architecture

(1) Stratix II ALM can implement a subset of 7-input functions
(2) Must have same logical function
# LUT Mapping to 6-LUT and ALM

<table>
<thead>
<tr>
<th>Output 1</th>
<th>Output 2</th>
<th>V-5 minimum # shared inputs</th>
<th>ALM minimum # shared inputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>5-LUT</td>
<td>5-LUT</td>
<td>5</td>
<td>2</td>
</tr>
<tr>
<td>5-LUT</td>
<td>4-LUT</td>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>5-LUT</td>
<td>3-LUT</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>4-LUT</td>
<td>4-LUT</td>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>4-LUT</td>
<td>3-LUT</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>3-LUT</td>
<td>3-LUT</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Fewer is Better
Stratix III 8-Input Fracturable LUT vs. Virtex-5 LUT-FF Pair

ALM Packs More Logic Efficiently for Higher Performance
Optimizing Power in Stratix III FPGAs
Meeting the Power Challenge

- Increased Performance
- 65 nm (Increased Leakage)
- Increased Density

Stratix III FPGAs Cut Power by 50% vs. 90 nm
## Lowest Power FPGA in the Industry

<table>
<thead>
<tr>
<th>Stratix III FPGA Power Reduction Technique</th>
<th>Lower Static Power</th>
<th>Lower Dynamic Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon Process Optimizations</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Selectable Core Voltage</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>(0.9 V or 1.1 V)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Programmable Power Technology</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Power-Optimized DDR Memory Interface</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Quartus II Software PowerPlay Power Analysis and Optimization</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>
Programmable Power Technology

Logic Array

Timing Critical Path

High-Speed Logic
Low-Power Logic
Programmable Power Technology

* Power mapping fully automated by Quartus II software based on timing constraints

High-Speed Logic
Low-Power Logic
Unused Low-Power Logic

High Performance Where You Need It, Lowest Power Everywhere Else
High Speed/Low Power

- Low-power mode for a tile results in
  - 60% reduction in static power
  - 5% reduction in dynamic power
  - ~20% increase in delay
    - Quartus II CAD system doesn’t use low-power mode on critical paths
    - No impact on system speed

- Tiles can be
  - Pair of logic array blocks (LABs)
  - RAM block
  - DSP block
High-Resolution Power Control

Stratix III FPGA (EP3SL340) has **8,050 tiles** for very high-resolution power/performance optimization.

Only a small percentage of high-speed tiles required to maintain design performance.

**Speed of the Fastest LABs, Power of the Slowest**
Automatic Programmable Power

1. Synthesis
2. Placement and Routing
3. Unused Tiles → Low Power
4. Timing Analysis
5. Tiles with Timing Slack → Low Power
6. Done? (Yes or No)

- All High-Speed Tiles
- Mostly Low-Power Tiles
Example: Power-Optimized RAM Mapping

- Default Option: Four 2Kx8 M9K RAMs
- Power-Efficient Option: Four 512x32 M9K RAMs with a 2:4 Decoder
Logic and Clock Power Optimization

- **Clock power reduction**
  - Stratix III hardware can shut down clock at 3 levels of tree
  - Automatic placement to reduce clock power

- **Power-driven placement and routing**
  - Minimize capacitance of high-toggling signals
  - Without violating timing constraints

Clocking Legal, Timing Optimized

Power Optimize

Group Clocks for Maximum Shutdown

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60% Lower Static Power (85°C)

Stratix II FPGA
- Typical high-performance design (1.1V)
- All low-power tiles (1.1V)
- Typical design (0.9V)

Stratix III FPGA
- Typical high-performance design (1.1V)
- All low-power tiles (1.1V)
- Typical design (0.9V)

Core Static Power (W) vs. Number of LEs
HardCopy III Structured ASICs - Designed for Low Power

- Structured ASIC – optimized architecture for power efficiency
- Unused logic and memory blocks not connected to power rail
- Unused clock trees and PLLs not powered
- Estimated power reduction from Stratix III FPGAs
  - >275 MHz: Up to 70%
  - >50 MHz and < 275 MHz: 30% to 70%
  - <50 MHz: Up to 30%
Summary

- Stratix III devices are the fastest FPGAs
  - Only FPGAs with a 600-MHz core clock speed
  - Supports high-speed DDR3 standard

- Stratix III FPGAs are, on average, one speed grade faster than Virtex-5 FPGAs
Thank You!