Develop a Display System Using New Low-Cost FPGAs
Agenda

- Display market dynamic and design challenge
- Key system diagrams
- Altera® Cyclone III is designed for display application
- Altera® design resources for display
- Conclusion
Trends in LCD TVs

- Larger (from 32” -> 50”)
- Higher resolution (from 480i -> 1080p)
- Wider color space (YCC -> xvYCC)

- Flexibility for future features
- Differentiation by own brand imaging algorithm
- Competes with plasma and projection
- Goal: home theatre experience
Display Design Challenges

- From SD to HD, from 32” to 60”, from YCC to xvYCC
  - → Need higher performance, low cost and lower power devices
  - → Higher flexibility for future upgrade

- How to differentiate your products?
  - → High competition in the market, a Me-too product only drive profit margin down
  - → Need to create value of imaging quality on video board to differentiate their products
  - → ASSP is not a solution here

- Should you use an FPGA or ASIC for a design?
  - Need to launch new features faster than competition
  - Uncertainty on market acceptance on new features
  - Short product life cycle
Key System Diagrams
First Low-Cost FPGA that Meets 1080p HDTV Performance Requirements

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FPGA Application in FPD

- Dynamic backlight control
- Dynamic gamma correction
- Image up/down scaling
- Frame rate conversion
- De-interlacing
- Video format conversion
- LCD panel re-timing
- ....and more
Cyclone III is Designed for Display Application
Unprecedented Combination

- **Low power**
  - TSMC 65-nm low-power (LP) process
  - Quartus® II software power-aware design flow
  - 120K logic elements (LEs) under ½ W
    - 1.4M equivalent ASIC gates

- **High functionality**
  - Densities ranging from 5K to 120K LEs
  - Up to 4 Mbits of embedded memory
  - Up to 288 embedded multipliers for digital signal processing (DSP)

- **Low cost**
  - First low-cost 65-nm FPGA
  - Free Quartus II Web Edition software
  - Prices starting as low as $4.00

*Turn Your Ideas Into Revenue Faster*
Meeting the Needs of Emerging High-Volume Applications

2002
- 2 – 20K logic elements (LEs)
- 295-Kbits embedded RAM
- DDR support
- Nios® embedded processor

2004
- 5 – 70K LEs
- 1.1-Mbits embedded RAM
- 150 18 x 18 multipliers for DSP
- DDR2 support
- Nios II embedded processor

2007
- 50% lower power vs. Cyclone ® II FPGAs
- 5 – 120K LEs
- 4-Mbits embedded RAM
- 288 18 x 18 multipliers for DSP
- Higher performance DDR2 support
- Nios II embedded processor

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Highest Functionality at the Lowest Cost

- Broadest range of low-cost FPGAs available
- Cyclone III FPGAs offer:
  - 2X the embedded memory
  - 2X the logic density
  - 2X the multipliers

over the competition
Typical Display Processing

Analog Source
- ADC (RGB)
- Digital Source
- PHY (MPEG, 1394, TMDS, LVDS)

ADC

Video ASSP
- LVDS

FPGA
- (Image Analysis Dynamic BLU control Image Enhancer)
- LVDS RS Mini-LVDS PPDS

BLU Driver board
- TTL

Panel

SDRAM
- MCU

Flash ROM

Improve ASIC/ASSP Picture Quality and Features for as Little as $4

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Enhanced LVDS Buffers

- Dedicated LVDS Output Buffers on the left and right banks
  - Increased performance, 840 Mbps
  - No external resistors required
- Improved LVDS Input Buffers on all banks
  - Increased performance, 875 Mbps
### LVDS Pairs Reference

<table>
<thead>
<tr>
<th>Package</th>
<th>Device</th>
<th>Total I/O</th>
<th>With dedicated output buffers</th>
<th>Without dedicated output buffers</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>E144</td>
<td>3C10</td>
<td>85</td>
<td>5</td>
<td>7</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td>3C16</td>
<td>67</td>
<td>3</td>
<td>4</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>3C25</td>
<td>65</td>
<td>4</td>
<td>2</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td>3C30</td>
<td>143</td>
<td>17</td>
<td>18</td>
<td>35</td>
</tr>
<tr>
<td>Q240</td>
<td>3C16</td>
<td>131</td>
<td>17</td>
<td>14</td>
<td>31</td>
</tr>
<tr>
<td></td>
<td>3C25</td>
<td>117</td>
<td>17</td>
<td>14</td>
<td>31</td>
</tr>
<tr>
<td></td>
<td>3C40</td>
<td>7</td>
<td>7</td>
<td>7</td>
<td>14</td>
</tr>
<tr>
<td>F256</td>
<td>3C10</td>
<td>173</td>
<td>21</td>
<td>36</td>
<td>57</td>
</tr>
<tr>
<td></td>
<td>3C16</td>
<td>151</td>
<td>19</td>
<td>24</td>
<td>43</td>
</tr>
<tr>
<td></td>
<td>3C25</td>
<td>139</td>
<td>18</td>
<td>24</td>
<td>42</td>
</tr>
<tr>
<td></td>
<td>3C40</td>
<td>111</td>
<td>17</td>
<td>14</td>
<td>31</td>
</tr>
<tr>
<td>F324</td>
<td>3C25</td>
<td>196</td>
<td>29</td>
<td>42</td>
<td>71</td>
</tr>
<tr>
<td></td>
<td>3C40</td>
<td>178</td>
<td>22</td>
<td>27</td>
<td>49</td>
</tr>
<tr>
<td></td>
<td>3C80</td>
<td>278</td>
<td>53</td>
<td>48</td>
<td>101</td>
</tr>
<tr>
<td>F484</td>
<td>3C16</td>
<td>329</td>
<td>66</td>
<td>62</td>
<td>128</td>
</tr>
<tr>
<td></td>
<td>3C40</td>
<td>314</td>
<td>58</td>
<td>56</td>
<td>114</td>
</tr>
<tr>
<td></td>
<td>3C55</td>
<td>310</td>
<td>61</td>
<td>62</td>
<td>123</td>
</tr>
<tr>
<td></td>
<td>3C80</td>
<td>278</td>
<td>53</td>
<td>48</td>
<td>101</td>
</tr>
<tr>
<td>F780</td>
<td>3C40</td>
<td>518</td>
<td>110</td>
<td>105</td>
<td>215</td>
</tr>
<tr>
<td></td>
<td>3C55</td>
<td>260</td>
<td>68</td>
<td>83</td>
<td>151</td>
</tr>
<tr>
<td></td>
<td>3C80</td>
<td>412</td>
<td>77</td>
<td>92</td>
<td>169</td>
</tr>
</tbody>
</table>
## Cyclone III: Supported I/O Standards

<table>
<thead>
<tr>
<th>Single-Ended I/O Standards</th>
<th>Max</th>
<th>Usage</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5V SSTL Class I and II</td>
<td>200 MHz</td>
<td>DDR SDRAM</td>
</tr>
<tr>
<td>1.8-V SSTL Class I and II</td>
<td>200 MHz</td>
<td>DDR/DDR2 SDRAM</td>
</tr>
<tr>
<td>1.8-V/1.5V/1.2-V HSTL I and II</td>
<td>167 MHz</td>
<td>QDR I/II SRAM</td>
</tr>
<tr>
<td>3.3-V PCI Compatible</td>
<td>66 MHz</td>
<td>Embedded</td>
</tr>
<tr>
<td>3.3-V PCI-X 1.0 Compatible</td>
<td>100 MHz</td>
<td>Embedded</td>
</tr>
<tr>
<td>3.3-V/2.5-V/1.8-V LVTTL</td>
<td>167 MHz</td>
<td>System Interface</td>
</tr>
<tr>
<td>3.3-V/2.5-V/1.8-V/1.5-V/1.2-V LVCMOS</td>
<td>167 MHz</td>
<td>System Interface</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Differential I/O Standards</th>
<th>Max</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVDS</td>
<td>875 Mbps</td>
<td>High-Speed Serial</td>
</tr>
<tr>
<td>RSDS</td>
<td>360 Mbps</td>
<td>High-Speed Serial</td>
</tr>
<tr>
<td>Mini-LVDS TX</td>
<td>440 Mbps</td>
<td>High-Speed Serial</td>
</tr>
<tr>
<td>LVPECL</td>
<td>500 MHz</td>
<td>High-Speed Serial</td>
</tr>
<tr>
<td>PCI Express*</td>
<td>2.5 Gbps</td>
<td>High-Speed Clocks</td>
</tr>
<tr>
<td>Serial RapidIO*</td>
<td>3.125 Gbps</td>
<td>Per Channel</td>
</tr>
</tbody>
</table>

*IP cores available, requires external PHY devices

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Video Line Buffering Application

Buffer eight lines of video in a mid-range Cyclone II device
Buffer eight lines of video in the smallest Cyclone III device

Line buffer requires 80 M4Ks or 40 M9Ks

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Volume price</td>
<td></td>
</tr>
<tr>
<td>$18.00</td>
<td>$4.00</td>
</tr>
</tbody>
</table>
## Enhanced PLLs for Displays

<table>
<thead>
<tr>
<th></th>
<th>Cyclone II</th>
<th>Cyclone III</th>
<th>Advantages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Outputs per PLL</td>
<td>3</td>
<td>5</td>
<td>Supports multiple data rates with up to 8 additional global clocks</td>
</tr>
<tr>
<td>Min - Max Frequency (MHz)</td>
<td>10 – 400</td>
<td>5 – 440</td>
<td>Supports higher data rates required by high definition displays</td>
</tr>
<tr>
<td>Dynamically Configurable</td>
<td>No</td>
<td>Frequency and Phase</td>
<td>Dynamically adjust for changing refresh rates</td>
</tr>
<tr>
<td>Cascadable</td>
<td>No</td>
<td>Yes</td>
<td>Increase PCB routing flexibility, reduce jitter</td>
</tr>
</tbody>
</table>
Reconfiguration enables display applications where the input frequency is unknown.

No Need for External Resistors

Performance Increase Up to 400 Mbps

PLL usage
## Cyclone III External Memory Support

<table>
<thead>
<tr>
<th>Memory Standards</th>
<th>C6 (MHz)</th>
<th>C7 (MHz)</th>
<th>C8 (MHz)</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Col I/O</td>
<td>Row I/O</td>
<td>Col I/O</td>
<td>Row I/O</td>
</tr>
<tr>
<td>DDR1 SDRAM</td>
<td>167</td>
<td>150</td>
<td>150</td>
<td>133</td>
</tr>
<tr>
<td>DDR2 SDRAM</td>
<td>200</td>
<td>167</td>
<td>167</td>
<td>150</td>
</tr>
<tr>
<td>QDRII SRAM</td>
<td>167</td>
<td>150</td>
<td>150</td>
<td>133</td>
</tr>
</tbody>
</table>

- All numbers are minimum frequencies achievable; maximum frequencies pending characterization
Cyclone III 65nm Low Power Technology

- Cyclone® III FPGAs deliver lower static and dynamic power consumption than Spartan-3 series families including the latest -3A and -3A DSP variants
  - Only Cyclone III FPGAs are designed on TSMC’s 65nm Low Power Process
  - Cyclone III static power is lower than Xilinx static power in Suspend mode at 85C Tj
  - Only Cyclone III FPGAs can take advantage of Quartus® II PowerPlay optimization technology to lower dynamic power up to 25%
Design Resources for Display
Quartus II Design Software

- Industry-leading software for performance and productivity
  - Supports all Cyclone III devices in free Web Edition
    - Including the EP3C120, largest FPGA in its class
- Key features
  - PowerPlay technology to reduce power up to 25 percent
  - TimeQuest timing analyzer for easy timing closure
  - DSP Builder to rapidly bring your DSP design into hardware
  - SOPC Builder to rapidly and easily build whole systems
# Video and Image Processing Suite

<table>
<thead>
<tr>
<th>Core</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Deinterlacer</td>
<td>Converts interlaced video formats to progressive video format</td>
</tr>
<tr>
<td>Color space converter</td>
<td>Converts image data between a variety of different color spaces</td>
</tr>
<tr>
<td>Scaler</td>
<td>Resizes and clips image frames</td>
</tr>
<tr>
<td>Gamma corrector</td>
<td>Performs gamma correction on a color space</td>
</tr>
<tr>
<td>Alpha blending mixer</td>
<td>Mixes and blends multiple image streams, including picture-in-picture (PIP)</td>
</tr>
<tr>
<td>Chroma resampler</td>
<td>Changes the sampling rate of the chroma data for image frames</td>
</tr>
<tr>
<td>2D filter</td>
<td>Implements a 3x3, 5x5, or 7x7 FIR filter on an image data stream to smooth or sharpen images</td>
</tr>
<tr>
<td>2D median filter</td>
<td>Implements a 3x3, 5x5, or 7x7 filter that removes noise in an image by replacing each pixel value with the median of neighboring pixel values</td>
</tr>
<tr>
<td>Line buffer compiler</td>
<td>Efficiently maps image line buffers to Altera on-chip memory</td>
</tr>
</tbody>
</table>

- 9 IP in one package to enable designers to kick start your own imaging algorithm!
Video Upconversion Datapath

- Entire datapath is assembled in DSP Builder

Diagram:

- Deinterlacer MegaCore®
- Chroma Resampler MegaCore
- Color Space Converter MegaCore
- Scaler MegaCore

Input Formats:
- 640 x 480 Interlaced 60 Hz YCbCr 4:2:2
- 640 x 480 Progressive 30 Hz YCbCr 4:2:2
- 640 x 480 Progressive 30 Hz YCbCr 4:4:4
- 640 x 480 Progressive 30 Hz RGB
- 1,024 x 768 Progressive 30 Hz RGB

Processing:

- Deinterlacer
- Chroma Resampler
- Color Space Converter
- Scaler

Output Formats:
- 640 x 480 Progressive 30 Hz YCbCr 4:4:4
- RGB

Interfaces:
- Two Avalon® Master Interfaces
- 8-bit Ready
- 8-bit Valid Data

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Nios II Embedded Processor

- Choose the *exact* set of CPUs, peripherals, and memory you need for your application
  - Achieve over 160 DMIPs of performance
  - Build custom instructions
  - Accelerate with hardware—C2H compiler automatically converts C subroutines into hardware for Nios II embedded processor

- Low cost
  - Integrate your peripherals and microprocessor into a single chip
  - Support for multiple processors in a single device
  - Implement a processor for $0.25 of logic on a Cyclone III FPGA

*Industrial’s Leading Soft-Core Processor*

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Complete Product Solution for Display

**MAX II use**
- Enhancements
- Bug Fixes
- Interface Bridging
- System Config

**MAX II benefits**
- Lowest Cost Per I/O Pin
- Instant-On, Non-Volatile
- Low Power Consumption
- Reprogrammable

**Cyclone III use**
- Image processing
- Timing controller
- Data arrangement
- Format conversion
- Interfaces

**Cyclone III benefits**
- Flexible, time-to-Market
- System integration
- FPD I/F built-in
- Memory I/F built-in
- Embedded Processor

**Stratix III use**
- Highest logic density
- Highest performance I/O (1.25G LVDS, 400Mhz DDRIII)

**Stratix III benefits**
- ASIC prototype
- HC migration

**HardCopy use**
- Similar to FPGA
- Structured ASIC

**HardCopy benefits**
- Risk reduction
- Time-to-market
- Improved performance
- Lower power
Cyclone III FPGA Starter Kit Available Now

- Full-featured FPGA board
  - Introduces the latest technology
- Cyclone III FPGA
  - Lots of Logic - 25K LEs
  - 608 kilobits of embedded RAM
  - 66 embedded 18 x 18 multipliers
  - 214 user I/O
- Built-in device programmer (USB)
- Memory Devices
  - SDRAM
  - SRAM
  - Flash
- Expandable with daughter cards through HSMC connector
- Part #: DK-START-3C25N/P

Get Your Design in Hardware Today
Microtronix ViClaro II HD Video Enhancement Development Platform

- Altera® EP2C35 device
- 32 bit DDR2 SDRAM
- HDMI Transmitter/Receiver
- Analog / Video Receiver
- Dual LVDS links
- Supports 720p/1080i/1080p 50/60HZ HDTV
LET IT WAVE Bandlet Transform Technology

- Let It Wave product
  - Built on Altera Stratix and Cyclone devices
  - Format conversion
    - Any input scaled to the desired resolution
    - Exceptional upconversion of SD sources to the display size
    - Delivering sharp and flicker-free images
  - Picture enhancement
    - Compression artefacts reduction
    - Advanced detail enhancement for clear images
  - Other features
    - Film mode detection, aspect ratio control
      ...

- Let It Wave Evaluation Kit and DVD
  - Available now for evaluation

“Superior Technology Award Recipient” at IBC 2006

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Breakthrough Picture Quality: Upconversion Example

Current state-of-the art

LET IT WAVE

“The Amazing Images Produced by The Let It Wave Upconversion Process Are Reaching The Ultimate Quality Point” -- Yves Faroudja
Other Altera® Display Application Resources

- Video and Image Processing Suite
  - Library of nine common video and image processing functions optimized for Altera FPGAs

- Video processing reference design

- Develop a Display System Using Low-Cost Cyclone III FPGAs QuickCast

- White papers
  - *Cyclone III FPGAs Enable a New Class of LCD HDTVs*
  - *A Flexible Architecture to Drive Sharp Two-Way Viewing Angle and Standard LCDs*
  - *Satisfy the Demand for Rapid Feature Enhancement in Consumer Display Products*

[www.altera.com/cyclone3-markets](http://www.altera.com/cyclone3-markets)
Conclusion
Conclusion

- The display evolution requires a high performance and flexibility solution to meet today market dynamics
- Cyclone III devices deliver low power, high performance, and low cost to enable customer innovation and fast time to market
- DSP Builder, Quartus® II design software, and development kits improve productivity
- Altera® display application resources and partner solution facilitate customers’ design
Thank You!
# Family Plan

<table>
<thead>
<tr>
<th>Device</th>
<th>LEs</th>
<th>M9K memory blocks</th>
<th>Total memory (Mbits)</th>
<th>18 X 18 Multipliers</th>
<th>PLLs</th>
<th>Global clocks</th>
</tr>
</thead>
<tbody>
<tr>
<td>EP3C5</td>
<td>5,136</td>
<td>46</td>
<td>0.4</td>
<td>23</td>
<td>2</td>
<td>10</td>
</tr>
<tr>
<td>EP3C10</td>
<td>10,320</td>
<td>46</td>
<td>0.4</td>
<td>23</td>
<td>2</td>
<td>10</td>
</tr>
<tr>
<td>EP3C16</td>
<td>15,408</td>
<td>56</td>
<td>0.5</td>
<td>56</td>
<td>4</td>
<td>20</td>
</tr>
<tr>
<td>EP3C25</td>
<td>24,624</td>
<td>66</td>
<td>0.6</td>
<td>66</td>
<td>4</td>
<td>20</td>
</tr>
<tr>
<td>EP3C40</td>
<td>39,600</td>
<td>126</td>
<td>1.1</td>
<td>126</td>
<td>4</td>
<td>20</td>
</tr>
<tr>
<td>EP3C55</td>
<td>55,856</td>
<td>260</td>
<td>2.3</td>
<td>156</td>
<td>4</td>
<td>20</td>
</tr>
<tr>
<td>EP3C80</td>
<td>81,264</td>
<td>305</td>
<td>2.7</td>
<td>244</td>
<td>4</td>
<td>20</td>
</tr>
<tr>
<td>EP3C120</td>
<td>119,088</td>
<td>432</td>
<td>3.9</td>
<td>288</td>
<td>4</td>
<td>20</td>
</tr>
</tbody>
</table>
## Package Offerings

<table>
<thead>
<tr>
<th>Device</th>
<th>E144</th>
<th>Q240</th>
<th>F256</th>
<th>U256</th>
<th>F324</th>
<th>F484</th>
<th>U484</th>
<th>F780</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.5 mm 22 x 22</td>
<td>0.5 mm 35 x 35</td>
<td>1.0 mm 17 x 17</td>
<td>0.8 mm 14 x14</td>
<td>1.0 mm 19 x 19</td>
<td>1.0 mm 23 x 23</td>
<td>0.8 mm 19 x19</td>
<td>1.0 mm 29 x 29</td>
</tr>
<tr>
<td>EP3C5</td>
<td>94</td>
<td>182</td>
<td>182</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EP3C10</td>
<td>94</td>
<td>182</td>
<td>182</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EP3C16</td>
<td>84</td>
<td>160</td>
<td>168</td>
<td>168</td>
<td></td>
<td></td>
<td>346</td>
<td>346</td>
</tr>
<tr>
<td>EP3C25</td>
<td>82</td>
<td>148</td>
<td>156</td>
<td>156</td>
<td>215</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EP3C40</td>
<td></td>
<td>128</td>
<td></td>
<td>195</td>
<td>331</td>
<td>331</td>
<td>535</td>
<td></td>
</tr>
<tr>
<td>EP3C55</td>
<td></td>
<td></td>
<td></td>
<td>327</td>
<td>327</td>
<td>377</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EP3C80</td>
<td></td>
<td></td>
<td></td>
<td>295</td>
<td>295</td>
<td>429</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EP3C120</td>
<td></td>
<td></td>
<td></td>
<td>283</td>
<td></td>
<td></td>
<td>531</td>
<td></td>
</tr>
</tbody>
</table>

Denotes vertical migration support

*Optimized to Offer the Highest Logic, Memory, Multiplier, and I/O Resources*