Display and DVR Application
Agenda

- Digital video recorder (DVR) market and display technical overview
- Key system diagrams
- Altera® solutions for DVR and display application
  - Reference designs and intellectual property (IP) cores
  - Tools and development kits
  - Devices
- Live demo
- Conclusion
Video Processing Trends

- Higher image capture and display resolutions
  - Increased consumer demand for digital content
  - Government conversion requirements
- Evolving compression techniques
  - M-JPEG $\rightarrow$ MPEG4 $\rightarrow$ H.264
- Needs for advanced system intelligence
Today’s Displays

CRT

Rear / Front Projection:
- CRT
- LCD
- DLP
- LCOS

LCD

PDP
- LCD
- DLP
- F-LCOS

< 40”

> 40”

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Trends in LCD TVs

- Larger (>50”)
- Higher resolution (1920 x 1080)
- >1 billion colors

- Flexibility for future features
- Competes with plasma and projection
- Goal: home theatre experience
Changing System Requirements...

Processing requirements increase

1. Over 2X more pixels need to be processed for each frame at 30 frames per second
2. Changes in encoding/decoding formats

Resolution increase
1280p x 720p
800p X 600p

Standard definition (SD) to high definition (HD) format
...Impacts to System Design

Resolution increase
1280p x 720p
800p X 600p

SD to HD format
Key System Diagrams
Display System Diagram

Composite DVD
Digital SD/HD
Memory stick
Digital video interface
...

Video Board
Scaler
Resolution control, contrast enhancement, edge enhancement, color enhancement, color compensation, ...

Driver Board
TCON
Driver IC Control signal generation

LVDS
RSDS Mini-LVDS
Panel Int’f

 CRT
Rear Projection
 LCD
PDP

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Digital Display Interfaces

- Transition minimized differential signaling (TMDS): Connection between PC and buffer board with DVI cable
- LVDS: Connection between buffer board and TCON board with FPC
- Reduced swing differential signaling (RSDS)/mini-LVDS: Connection between TCON board and column driver board with FPC
DVR System: Hardware Compression

- **SDRAM**
- **Altera FPGA**
- **Multi-Channel Video QUAD/Multiplexer Controller**
- **Playback**
- **Video Encoder**
- **Recorder**
- **SDRAM**
- **MPEG4 or H.264 Hardware Compression**
- **CPU (Nios® Processor)**
- **PCI or PCI Express**
- **IDE**
- **SATA**
- **Ethernet**
- **Video Server and Network DVR**
- **PC-Based DVR**

**Embedded DVR**

**Audio ADC**

**CCIR656**

**I2S**

**4/9/16 Channels**

**Video Decoder**

**4/9/16 Channels**

**Embedded DVR**

**Audio ADC**
PCI-Based DVR: PC Software Compression

- PCI or PCI Express Bridge
- SDRAM
- H/V Scalar
- DMA Controller
- DMA Controller
- FIFO

4/9/16 Channels

- Video Decoder
- Audio ADC
- CCIR656
- I2S
- Altera FPGA

PCI Bus
IP Examples – Video

I/O and system
- PCI Express
- Serial RapidIO™ standard
- Electro-magnetic interference filter (EMIF) interface
- Asynchronous Serial Interface (ASI)
- Serial digital interface (SDI)
- ATA HDD (Nuvation)
- MPEG-2 transport
- 10/100/1000 Ethernet
- DDR/DDR2 controller

Pre-/post-processing
- Scaler
- Deinterlacer
- 2D finite impulse response (FIR) filter
- 2D median filter
- Color space converter
- Chroma resampler
- Gamma corrector
- Alpha blender
- Highest quality HDTV upconversion (Let It Wave)
- Advanced encryption standard (AES)/data encryption standard (DES)/Sha-1 Encryption (CAST)

Compression
- H.264 MP, HP (ATEME)
- H.264 BP (4i2i, CAST, W&W)
- H.264 CABAC/CAVLC (ATEME)
- H.264 Loop Filter (ATEME)
- MPEG-4 SP/ASP (CAST, Barco)
- JPEG (CAST, Barco)
- JPEG2000 (CAST, Barco, BroadMotion)

Video and Image Processing Suite
## Video and Image Processing Suite

<table>
<thead>
<tr>
<th>Core</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Deinterlacer</td>
<td>Converts interlaced video formats to progressive video format</td>
</tr>
<tr>
<td>Color space converter</td>
<td>Converts image data between a variety of different color spaces</td>
</tr>
<tr>
<td>Scaler</td>
<td>Resizes and clips image frames</td>
</tr>
<tr>
<td>Gamma corrector</td>
<td>Performs gamma correction on a color space</td>
</tr>
<tr>
<td>Alpha blending mixer</td>
<td>Mixes and blends multiple image streams, including picture-in-picture (PIP)</td>
</tr>
<tr>
<td>Chroma resampler</td>
<td>Changes the sampling rate of the chroma data for image frames</td>
</tr>
<tr>
<td>2D filter</td>
<td>Implements a 3x3, 5x5, or 7x7 FIR filter on an image data stream to smooth or sharpen images</td>
</tr>
<tr>
<td>2D median filter</td>
<td>Implements a 3x3, 5x5, or 7x7 filter that removes noise in an image by replacing each pixel value with the median of neighboring pixel values</td>
</tr>
<tr>
<td>Line buffer compiler</td>
<td>Efficiently maps image line buffers to Altera on-chip memory</td>
</tr>
</tbody>
</table>
VIP Upconversion System

- National Television System Committee (NTSC) Video Input: Composite Input on Video Daughtercard
- Video Upconversion
- Triple Buffer
- HD Video Output: VGA Controller
- DDR II SDRAM
- DSP Builder
- SOPC Builder
Video Upconversion Datapath

- Entire datapath is assembled in DSP Builder
Display Application Resources

- Video and Image Processing Suite
  - Library of nine common video and image processing functions optimized for Altera FPGAs

- Video processing reference design

- Low-Cost FPGA Starter Kit, Cyclone III Edition

- Microtronix ViClaro II HD Video Enhancement Development Platform

- *Develop a Display System Using Low-Cost Cyclone III FPGAs* QuickCast

- White papers
  - *Cyclone III FPGAs Enable a New Class of LCD HDTVs*
  - *A Flexible Architecture to Drive Sharp Two-Way Viewing Angle and Standard LCDs*
  - *Satisfy the Demand for Rapid Feature Enhancement in Consumer Display Products*

www.altera.com/cyclone3-markets
Video and Image Processing Resources

- Video and image processing IP
  - Library of nine common video and image processing functions from Altera
  - Compression IP available from Altera partners such as ATEME, Barco, 4i2i, and CAST

- Video processing reference design

- Video training course
  - Advanced DSP design: using FPGAs to architect and optimize a video and image processing system

- Low-cost FPGA Starter Kit, Cyclone III Edition

- Video daugtercard

- Design Video and Image Processing Systems with Low-Cost Cyclone III FPGAs QuickCast

- White papers
  - Video and Image Processing Design Using FPGAs
  - Video Surveillance Implementation Using FPGAs
  - Medical Imaging Implementation Using FPGAs
Graphics Processor Platform

- Nios II Embedded Processor
- Graphics Acceleration DAVE2DT
- Host Interface
- Video In
- Avalon Bus Fabric
- SDR/DDR Interface
- DMA-FIFO
- Alpha Blending
- TFT Timing

To TFT Display
## Graphics Solutions Selector Guide

<table>
<thead>
<tr>
<th>Altera Graphics Solutions</th>
<th>Lowest cost</th>
<th>Low-end</th>
<th>Mid-range</th>
<th>High-end</th>
<th>SOC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Applications</td>
<td>RSE Rear-view camera</td>
<td>RSE Cluster Rear-view Night vision Low-cost Navi</td>
<td>High-end Cluster Navigation</td>
<td>High-end Navigation Game Console additional functions</td>
<td>Multimedia Controller High-end graphics Audio Codec and other functions</td>
</tr>
<tr>
<td>Target Device</td>
<td>EP1C3T100 EP2C5T144</td>
<td>EP2C5F256</td>
<td>EP2C8F256</td>
<td>EP2C20F256</td>
<td>HC210W</td>
</tr>
</tbody>
</table>

### Graphics Feature List

- **Layering**: Yes
- **Alpha Blending (layer alpha, pixel alpha)**: Yes
- **Clipping / Resizing**: Yes
- **Video input**: Yes
- **Picture-in-Picture**: Yes
- **Colour Depth**: Yes
- **Anti-aliasing**: on Host Micro
- **Line Drawing**: on Host Micro
- **Polygon Drawing**: on Host Micro
- **Circles & Ellipses**: on Host Micro
- **Quadratic and Cubic Bézier**: on Host Micro
- **Bitmap BLT**: on Host Micro
- **Multiple render-attributes**: on Host Micro
- **Multiple Bitmap Formats**: on Host Micro
- **HW Support for Matrix Computation**: -
- **Graphics Library & OpenGL Compliance**: on Host Micro
- **3D Graphic rendering engine**: -
- **RGB Digital Output**: Yes
- **LVDS Output**: Yes
- **Memory Interfaces (SDR, DDR, Flash)**: Yes
- **Flexible Host Interfaces**: Yes

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Graphics Hardware Acceleration

- D/AVE (Display Controller and Accelerated Vector Engine)
  - Provided by TES (former ThalesEE)
  - A specialized graphics acceleration hardware
  - Innovative, vector-based rendering engine
  - High render quality (sub-pixel and anti-aliasing)
  - Low resource consumption
  - Flexible design, easy to parallelize, easy to add new functionality
  - Low memory bandwidth consumption
  - Key features:
    - Blit operation in D/AVE 2DT-S (direct blit, stretch blit, transparency, bilinear filtering, per pixel alpha, coloring, antialiasing)
    - Lines (arbitrary width, round endpoints, truncated endpoints, alpha gradients, soft edges (blurring))
    - Polygons (triangles and quadrangles, alpha gradients, soft edges (blurring), per edge controls for anti aliasing)
    - Circles and ellipses (all conic sections, filled or with arbitrary width, arcs of 0° -360°, soft edges, alpha gradients)
    - Quadratic and cubic Bézier (approximate by circle arcs, arbitrary width, round or truncated endpoints, outlines blurring, alpha gradients)
    - Render-attribute: color, pattern, texture
    - Supported bitmap formats: Alpha8 (8Bit), Alpha8In32 (8Bit), RGB 555 (16Bit), RGB 565 (16Bit), ARGB 4444 (16Bit), RGB 888 (32Bit), ARGB 8888 (32Bit)
Multimedia Solutions Roadmap

- **Low-end Graphics Controller**
  - EP2C5

- **Mid-range Graphics Controller**
  - EP2C8

- **High-end Graphics Controller**
  - EP2C20

- **Multimedia Controller**
  - HardCopy® structured ASIC

- **Performance/Features**
  - Low-end Navigation
  - Navigation Cluster
  - Night Vision
  - Rear-view
  - High-end Navigation Cluster
  - High-end Navigation
  - High-end CODEC
  - Game
  - 3D

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The Significance of Power

- Challenges
  - Thermal management
  - Fixed power budgets
  - Battery life

- Cyclone III FPGAs allow you to do more with less power

Increase functionality while reducing power
Display Application Challenges

Display application examples
- LCD and plasma displays and projectors
- DVD player/recorder
- Automotive/navigation displays
- Medical and industrial imaging

High Functionality
- Higher video-rate processing for standard-definition (SD) to high-definition (HD) conversion
- Larger display panels require image enhancement to reduce/eliminate digital video noise artifacts
- Demand for upgrade path to next-generation features (e.g. video, 3D rendering, picture-in-picture, enhanced on-screen display (OSD))

Low Cost
- Single graphics controller solution to address range of display sizes, external memory types, feature sets
- Declining profit margins over product lifecycle
- ASIC design cycles do not meet time-to-market requirements

Low Power
- Battery life for portable applications
Universal, Flexible, and Scalable Display Controller

Integrate the exact display functions you need

Add a custom video and image processing algorithm

Support for multiple simultaneous displays in every resolution, including non-standard

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Video and Image Processing Challenges

Video and imaging application examples

• Video surveillance
• Video conferencing
• Medical/industrial/military imaging
• Automotive infotainment

High Functionality
• Video standards continue to evolve, driving higher data rates (e.g. H.264)
• Processing requirements are outpacing digital signal processing (DSP) performance

Low Cost
• Expensive or multiple DSP processors required for HD class video
• ASIC design cycles do not meet time-to-market requirements

Low Power
• Thermal dissipation can interfere with sensitive charge-coupled device (CCD) image capture devices
Video Line Buffering Application

Buffer eight lines of video in a mid-range Cyclone II device

Buffer eight lines of video in the smallest Cyclone III device

Line buffer requires 80 M4Ks or 40 M9Ks

<table>
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<tr>
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<tbody>
<tr>
<td>Volume price</td>
<td></td>
</tr>
<tr>
<td>$18.00</td>
<td>$4.00</td>
</tr>
</tbody>
</table>

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Enable Low-Cost H.264 Encoding

Processing intensive blocks

Implement SD H.264 Encoder in a Single Device for Under ¼ W and $5 per Channel
Tools and Development Kits
System Integration Solution

Create Design Blocks

IP

Model-Based Design

‘C’-Based Design

HDL Entry

entity par_fr is
port (i0_o_p : out std_logic_vector(15 downto 0);
i0_i_p : in std_logic_vector(15 downto 0);
clock : in std_logic;
reset : in std_logic
);
end entity;

Integrate System

Embedded Software Development

Nios II IDE

Including

SOPC Builder
Concept to System in Minutes

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Another tool that extends FPGA design to higher abstraction level

Brings software productivity to hardware design

Accelerates time-critical C code
- Converts ANSI C subroutines to hardware accelerators
- **Automatically** adds accelerators to a Nios II system

Tightly integrated into Nios II embedded processor design environment
Cyclone III Base Kits

Available April 2007 $199

Available October 2007 $695

Cyclone III FPGA Starter Kit
- EP3C25F324
- HSMC connector
  - Allows daughtercard expansion
- On-board memories:
  - 256-Mbit DDR
  - 1-Mbyte sync SRAM
  - 16-Mbyte flash

Cyclone III Dev Kit
- EP3C120F780
- 2x HSMC connectors
  - Allows daughtercard expansion
- 10/100/1000 Ethernet
- On-board memories:
  - 256-Mbit DDR2
  - 8-Mbyte sync SRAM
  - 64-Mbyte flash

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Live Demo

Video Image Processing Suite reference design:

- Video and image processing upconversion example design demonstrates upconversion from a SD video stream in National Television System Committee (NTSC) format to a HD output resolution (1024 × 768).
Conclusion

- Cyclone III devices deliver low power, high performance, and low cost to enable customer innovation.
- DSP Builder, Quartus® II design software, and development kits improve productivity.
- Display and video image processing application resources facilitate customers’ design.