High-Performance Digital Signal Processing (DSP) Applications with Serial RapidIO Standard
Agenda

- High-performance DSP applications
- Serial RapidIO™ review
- Altera® Serial RapidIO solution
- Altera Serial RapidIO demo
Growing Demand for MIPS and Memory Bandwidth

- Growth Drivers
  - Algorithm Complexity
  - Resolution
  - Real Time
  - Multiple Users

Application Requirements

Digital Signal Processors

Time

DSP MIPS and Memory Bandwidth
## DSP vs. FPGA Comparison – 1

<table>
<thead>
<tr>
<th></th>
<th>DSP</th>
<th>FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Advantages</strong></td>
<td>High clock rate</td>
<td>High number of instructions/clock</td>
</tr>
<tr>
<td></td>
<td>Rapid software development in C++</td>
<td>High number of multipliers</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High bandwidth flexible I/O and memory connectivity</td>
</tr>
<tr>
<td><strong>Disadvantages</strong></td>
<td>Limited number of instructions/clock</td>
<td>Longer development time</td>
</tr>
<tr>
<td></td>
<td>Limited number of multipliers</td>
<td>Typically lower clock rates</td>
</tr>
<tr>
<td></td>
<td>Limited memory and device connectivity</td>
<td></td>
</tr>
</tbody>
</table>
## DSP vs. FPGA Comparison – 2

<table>
<thead>
<tr>
<th>Functions</th>
<th>DSP</th>
<th>FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum clock rate</td>
<td>1 GHz</td>
<td>370 MHz</td>
</tr>
<tr>
<td>Maximum number of multipliers</td>
<td>4 (16-bit X16-bit)</td>
<td>Over 700 18-bit X 18-bit (384 HW + 300 LE) or over 1400 9-bit X 9-bit¹</td>
</tr>
<tr>
<td>Maximum number of instructions/clock</td>
<td>4 or 8</td>
<td>100s to 1000s</td>
</tr>
<tr>
<td>Ease of programming</td>
<td>C,C++ software flow</td>
<td>HDL hardware flow</td>
</tr>
<tr>
<td>I/O flexibility</td>
<td>Limited</td>
<td>Flexible</td>
</tr>
<tr>
<td>Memory management</td>
<td>Built-In</td>
<td>Manual</td>
</tr>
<tr>
<td>Memory bandwidth</td>
<td>1-Gbps SDRAM</td>
<td>9.5-Gbps DDRII²</td>
</tr>
<tr>
<td>Power consumption (for high-end processing devices)</td>
<td>Low per device (high per computation)</td>
<td>High per device (low per computation)</td>
</tr>
</tbody>
</table>

---

(1) Multipliers Can Be Implemented Using Hardware (HW) Based Multipliers & Logic Element (LE) Based Multipliers.
(2) Other Memory Interfaces are Supported Including Single Data Rate, Double Data Rate, RLDRAMII, QDR & QDRII²
Datapath Processing Architecture Options

Performance (MMACs/sec)

Stand-Alone Processor  Processor Array  Processor + FPGA Coprocessor  Dedicated Hardware Architecture

© 2007 Altera Corporation—Public
Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation
Example: Wireless Tester

Analyzer Card (Rx)
- Demodulate and FEC
- Pattern Detector
- Memory Controller

Generator Card (Tx)
- Modulate and FEC
- Pattern Generator
- Memory Controller

RF Card
- Down Converter
- LNA
- RF
- PA
- UP Converter
- A/D
- D/A

Control Card
- Host CPU
- Control Logic
- Glue Logic

Backplane
Example: WiMAX Channel Card
Example: WiMAX Channel Card

- A/D
- D/A
- Digital I/F
- DUC/DDC
- DPD
- CFR
- Glue Logic
- RF Card
- Baseband Processing
  (WCDMA/cdma2000/WiMAX)
- Glue Logic
- Channel Card
- Multiplexer/De-Multiplexer
- Host uP
- IP Proc
- Host CPU
- Control Logic
- Glue Logic
- Control Card
- Clock Generator
- GPS Receiver
- Timing Card
- Glue Logic
- Switch Card
- Switch I/F
- BSC/RNC Interface
- IP/ATM Interface
- Glue Logic

PA
LNA

© 2007 Altera Corporation

Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation
Serial RapidIO Review
Interconnect Technology Review

**Interconnect Use**

- **LAN/WAN**
  - Characteristics: Ethernet, IPv4/IPv6, 48-bit MAC Address

- **Traffic-Managed Fabric**
  - Characteristics: Hundreds of classes, millions of flows, end-to-end flow control, interworking, scalable

- **Switched Interconnect**
  - Characteristics: Message passing, architectural/topological independence, one flow, protocol tunneling

- **Serial Local Bus**
  - Characteristics: Serialized Input/Output Transactions/DMA

- **Parallel Local Bus**
  - Characteristics: Parallel Input/Output Transactions/DMA

**RapidIO**
RapidIO Hierarchy

Logical Specification
- I/O System
- Message Passing
- Globally Shared Memory
- Flow Control
- Data Plane Extensions

Transport Specification
- Common Transport Spec

Physical Specification
- 8,16 Parallel
- 1x/4x Serial
- Future Physical Specs

Layered Architecture Limits Impact on Software

Inter-Operability Specification

Impact on Software
Traditional Interconnect Architecture

Host Subsystem
- Host Processor
- Bridge
- Memory
- Proprietary Bus

I/O Control Subsystem
- Control Processor
- ASIC/FPGA
- Bridge
- Memory
- Proprietary Bus

DSP Farm
- Proprietary Bus
- DSP
- DSP
- DSP
- DSP

Communications Subsystem
- Comm Processor
- Memory
- Network Processor
- TDM, GMII, Utopia
- To Data Path Switch Fabric

PCI Subsystem
- PCI to PCI Bridge
- Legacy
- PCI

PCI Backplane

© 2007 Altera Corporation—Public
Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation
Typical Application

**DSP Farm Switch and Backplane Interconnect**
Typical Application

DSP Coprocessor

© 2007 Altera Corporation—Public
Altera, Stratix, Arria, Cyclone, MAX, HardCopy, Nios, Quartus, and MegaCore are trademarks of Altera Corporation
Altera Serial RapidIO Solution
Altera Stratix II GX RapidIO Solution

- RapidIO MegaCore® Version 6.1
- Compliant with RapidIO Trade Association, RapidIO Interconnect Specification, Revision 1.3
- Physical layer features
  - 1x/4x serial
    - Stratix® II GX support, including 1x and 4x up to 3.125 Gbps
    - Cyclone® II, Stratix II, Stratix III, and HardCopy® II support with an XGMII-like interface to a high-speed full-duplex, serializer / deserializer (SERDES) transceiver
  - 8-bit parallel
- Transport layer features
  - Supports multiple logical layer modules
  - Supports 8-bit device identities (IDs)
  - Device IDs, addressable CARs, and CSRs eliminate hop-count handling and CRC recomputing
- Logic layer features
  - Maintenance master and slave logical layer module
  - I/O master and slave logical layer module
  - Doorbell support
- PCI Express development kit expansion via HSMC connectors to AMC module
- SRIO loopback example design available based on the signal integrity kit
- Other IP vendors: Mercury Computers, GDA Technologies, Jennic, Preasum
SRIO Stratix II GX Characterization

- SRIO I/O (PMA) specifications have evolved
  - Currently identical to XAUI @ 3.125 Gbps
  - Currently identical to Gigabit Ethernet @ 1.25 Gbps and 2.5 Gbps

- Stratix II GX passes SRIO characterization spectacularly at 3.125 Gbps

- The XAUI and SRIO characterization report now available
Interoperability

- Stratix II GX with Altera MegaCore interoperability with TI DSP device via SRIO
  - Stratix II GX signal integrity (SI) board to TI DSP 6455 board via an SMA breakout board

<table>
<thead>
<tr>
<th>Number of Lanes</th>
<th>Baud Rate (Gbaud)</th>
<th>Internal Data Path Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>X1</td>
<td>1.25</td>
<td>32</td>
</tr>
<tr>
<td>X1</td>
<td>2.5</td>
<td>32</td>
</tr>
<tr>
<td>X1</td>
<td>3.125</td>
<td>32</td>
</tr>
<tr>
<td>X4</td>
<td>2.5</td>
<td>64</td>
</tr>
<tr>
<td>X4</td>
<td>3.125</td>
<td>64</td>
</tr>
</tbody>
</table>

- Interoperability with IDT switch x1 @ 3.125 Gbps
- Bittware AMC board with Stratix II GX interoperability with TI DSPs via Tundra passed
# Stratix II GX FPGA-based Serial RapidIO Solution

<table>
<thead>
<tr>
<th>Item</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stratix II GX FPGA</td>
<td>✔</td>
</tr>
<tr>
<td>IP core (x1, x4 serial, x8 parallel)</td>
<td>✔</td>
</tr>
<tr>
<td>Development kit</td>
<td>✔</td>
</tr>
<tr>
<td>Reference designs</td>
<td>✔</td>
</tr>
<tr>
<td>Device characterization report</td>
<td>✔</td>
</tr>
<tr>
<td>System validation report</td>
<td>✔</td>
</tr>
<tr>
<td>Additional interoperability (Texas Instruments)</td>
<td>✔</td>
</tr>
</tbody>
</table>
Summary

- Serial RapidIO has become the interface of choice for high-performance DSP applications
- Altera offers complete, easy-to-use Serial RapidIO solutions
  - Arria™ GX FPGAs for mainstream applications
  - Stratix II GX FPGAs for high-performance systems
- Low-risk, hardware-verified solutions
  - Stratix II GX interoperability with Texas Instruments
  - Development boards

Fastest Time-To-Market with Reliable RapidIO Solutions
Serial RapidIO Demo