Xilinx Solutions for Next Generation SONET/SDH Networks

Xilinx, Inc.
Agenda

• Telecom today and SONET / SDH
• Data over SONET / SDH technologies
• Xilinx solutions for next generation SONET / SDH
Telecom Today & SONET/SDH

- Fiber-optical transport system (L1)
  - Synchronous Optical NETwork and Synchronous Digital Hierarchy

- Scalable performance
  - 155Mbps (OC3/STM1) to 40 Gbps (OC192/STM64) and beyond

- Widely deployed
  - In over 95% of telecom optical infrastructure
  - Multiple, global equipment vendors

- Supports an array of traffic, but ideal for voice and delay sensitive traffic
Future of SONET/SDH

• Carriers want to keep SONET due to its reliability, standardization, flexibility, QoS, manageability, scalability
• Carrier investment and SONET proliferation is continuing in the edge and metro area
• SONET/SDH variants needed for efficient data transport
• Multi-Service Provisioning Platforms (MSPP)
  – Combines various functionalities and protocol support into a single chassis with SONET/SDH, Ethernet, Fibre Channel, IP, etc.
  – Built for the Metro Edge Networks to alleviate metro-bottleneck, save rack space, power, and $$$
• Key opportunity: Data (Ethernet, FC, etc.) over SONET/SDH
Data over SONET / SDH Issues

• SONET has fixed Synchronous Payload Envelopes (SPE)
  – How to efficiently transport mis-matched frames?

• Inefficient, inflexible & expensive scheme
  – Mapping into SONET is line rate/ bandwidth mismatched
    • Mapping 10 Mbps Ethernet into SONET requires the entire STS-1 (payload size of 48.384 Mbps): 20.7% utilized
    • Gig Ethernet requires an entire OC-48 (2.5 Gbps): 41.7% utilized

• Inflexibility due to burst nature of Ethernet (IP traffic) and Fibre Channel frames
Today’s Metro Area Network

New and Legacy Technologies

Metro Backbone
SONET, ATM, PoS, DWDM

Internet Backbone

Metro Aggregation
T1, T3, WDM, Ethernet

Broadband Access
Cable, DSL, Wireless

Metro Access
T1, ATM, FR, Ethernet

Data Center
Storage & Servers

Source: RPR Alliance
Client SAN Requirements

• Different packet types coexist on the same SAN
  – Metro equipment will have a mixture of port types
• For example
  – Fiber Channel from storage arrays
  – iSCSI/Ethernet from ESAN/LAN
  – ESCON for legacy data centers
• In the future:
  – Add video, and other native storage formats
  – 8B10B encoding is a key requirement
LAN Technology for SAN

• TCP/IP is the predominant data transport protocol
  – iSCSI is SCSI commands encapsulated by TCP/IP
  – Resilient to latency variation and packet loss
    (1-2% packet loss* is typical across Internet)
• FC is the storage data transport protocol
  – Delivers in-order, loss-less data
  – Credit buffering provides end-to-end flow control
  – Sensitive to latency

*www.internetweather.com - independent source of IP network performance
Ethernet over SONET (EoS)

- EoS collectively represents a group of industry (ITU) specs that have been developed for optimal transport of Ethernet over SONET/SDH
  - Very cost-effective
  - Allows bandwidth to be shared among several Ethernet ports

- Using EoS with VC a GE channel can be built (24 STS-1’s concatenated) while the unused portion of the OC-48 bandwidth can be deployed for other Ethernet or TDM services
Modern SONET Technology

• Generic Framing Procedure (GFP) - G.7041
  – Provides a standard mapping of Level 1-2 (Link Layer) protocols into SONET/SDH (or OTN)

• Virtual Concatenation (VCAT) - G.707
  – Enables SONET streams to be multiplexed together in arbitrary configurations (create right-sized ‘pipes’)

• Link Capacity Adjustment Scheme (LCAS) - G.7042
  – Enables SONET streams to be dynamically re-provisioned to meet bandwidth requirements
Generic Framing Procedure/Protocol (GFP)

- GFP joint standardization: ANSI and ITU-T (G.7041)
- Protocol for mapping packet data into an octet-synchronous transport like SONET
  - Protocol-agnostic frame delineation (L2 & higher) & encapsulating mechanism for transporting packets
  - Robust & efficient packet transport
- GFP frame = GFP header + GFP payload
# GFP Mapping to SONET/SDH

<table>
<thead>
<tr>
<th>IP Data Services</th>
<th>10GE</th>
<th>ATM</th>
<th>PPP (POS)</th>
<th>Ethernet</th>
<th>RPR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage Services</td>
<td>GE, ESCON, FC, FICON</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Future Services</td>
<td>Transparent GFP</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lambda Services</td>
<td>OTN</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
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</table>

- Virtual Concatenation
- SONET/SDH
- DWDM
Frame Mapping

- Client (Ethernet) frames are stripped of 8B10B encapsulation and Inter-Frame Gap (IFG)
- Client frames are encapsulated in GFP frames
Transparent Mapping

- Client symbol stream is encapsulated into fixed-size GFP frames. Rate adaptation is required.
- Opacity! Must insert/remove idles. Also latency...
Data Encapsulation Evolution

Client Data

ATM Cells

PPP/HDLC

GFP
Transport Over SONET

VCAT enables right-sized pipes
Efficient use of VC

Source: Tellabs
Dynamic Reprovisioning of SONET/SDH Bandwidth

• Link-Capacity Adjustment Scheme (LCAS)
  – Supplement to VC function for dynamic bandwidth adjustment
  – Allows designers to adjust capacity on a real-time basis
  – Carrier & equipment manufacturers can adjust the amount of STS-1s provided in a group dynamically for network conditions

• Link-Access Procedure for SDH (LAPS)
  – Defined as a type of HDLC that includes data link service and protocol spec used in transporting IP packets over SDH
  – Provides a point-to-point unacknowledged connectionless service over SDH
  – Enables encapsulation of IPv6, IPv4, PPP & other higher-layer protocols
Programmable MSPP Line Card

- O/E
- Physical Layer Transceiver
- Framer MAC
- NPU
- Memory
- Backplane/Switch Fabric
- Control Plane
Xilinx Solutions
Next-Gen RocketIO™ Multi-Gigabit Serial Technology

Next-Gen Memory Technology

Next-Gen Clocking & Clock Mgmt Technology

Next-Gen SelectIO Technology

Embedded Tri-Mode Ethernet MAC

Next-Gen PowerPC™ Processing Technology

Virtex-4 FX Silicon Floorplan
# V-4 Benefits for MSPP

<table>
<thead>
<tr>
<th>Feature</th>
<th>VIRTEX-II PRO</th>
<th>VIRTEX-II PRO X</th>
<th>VIRTEX VX</th>
<th>RocketPHY</th>
<th>Benefit</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA Fabric</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Allows integration of processing components (MAC/Framer), and customization</td>
</tr>
<tr>
<td>Configurable PCS</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Allows a single line card to support multiple data protocols</td>
</tr>
<tr>
<td>x16 and x20 support</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Allows support of SONET / SDH traffic</td>
</tr>
<tr>
<td>SONET Jitter compliance</td>
<td>OC-48</td>
<td>OC-12</td>
<td>OC-48</td>
<td>OC-192 G.709</td>
<td>Direct interface to other devices, reduces component count</td>
</tr>
</tbody>
</table>
Xilinx IP Solutions for MSPP

- SPI-3
- SPI-4.2
- GFP-F
- GFP-T
- 1G Base-x
- 10GE
- 1 & 2 Gbps FC
- FICON
- ESCON
- 1GE
- 10GE
- OC-48
- OC-192
- VC/LCAS
- SPI-3
- SPI-4.2

Ethernet/FC
SFP/GBIC Optical Module
PHY Layer
CPCS
MAC
GFP
SONET Framer
PMD
Optics
MGT (622-11.1G)
OC-48, OC-192, VC/LCAS
SPI-3, SPI-4.2
GFP-F, GFP-T
1G Base-x, 10GE, 1 & 2 Gbps FC, FICON, ESCON

GFP IP Core: Highlights

- Fully compliant with ITU-T G.7041 GFP recommendation
- Configurable for frame-mapped, transparent, or Mixed Mode
  - Individually optimized for OC-48 or OC-192 applications
- Supports MANY different protocols
  - Frame: Ethernet, PPP, RPR
  - Transparent: Gigabit Ethernet, Fibre Channel, FICON, ESCON, DVB ASI
- Supports up to 10 unique channels
  - Multi-line / Multi-protocol applications
  - MSPP’s, e.g., 10x 1GE => OC-192
GFP IP Core

- Xilinx standard LocalLink interfaces
  - easy system integration
- Map & Unmap cores delivered independently
  - Enables separate ingress and egress paths/devices
- Dynamic reconfiguration through host interface
  - No line-card power-down

<table>
<thead>
<tr>
<th>Speed</th>
<th>Mode</th>
<th>Slice</th>
</tr>
</thead>
<tbody>
<tr>
<td>OC-48</td>
<td>Frame-mapped</td>
<td>2000</td>
</tr>
<tr>
<td>OC-192</td>
<td>Frame-mapped</td>
<td>4000</td>
</tr>
<tr>
<td>OC-192</td>
<td>Frame/Transparent</td>
<td>2000</td>
</tr>
</tbody>
</table>
GFP: Buffer Manager Ref Core

- Frame buffering
  - Store and forward on a per-channel basis
  - Round robin between N channels
  - Clock adaptation (N client clks to one system clk)
  - Applicable to both GFP-F and GFP-T
- Utilize on-chip or off-chip RAM
- Local Link for easy system integration
SPI-4.2 IP Core

- 22% smaller FPGA implementation in V-4
  - 3900 slices for fully-compliant (OIF-SPI4-02.1) DPA solution
- Up to 1-Gbps/pin data rates
  - 311-Mhz DDR minimum for 10-Gbps
  - NPU SPI-4.2 interfaces up to 500-Mhz DDR (16-Gbps)
- Complete pinout flexibility
  - NOT pinlocked
- Support for multiple cores
  - Up to 4(+) SPI-4.2 interfaces in a single Virtex-4 device
- Differential global clock implementation
  - Improved system margins for designers
SPI-4.2 IP Core

- **Embedded DPA**
  - Utilizes dedicated source synchronous resources in Virtex-4

- **Industry leading payload efficiency**
  - No idle insertions, supports back-to-back small packets

- **Independent Sink & Source cores**
  - Enables separate ingress and egress paths/devices

Most extensive industry-proven hardware interoperability

<table>
<thead>
<tr>
<th>Core Resources</th>
<th>Dynamic Alignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Virtex-4 Slices</td>
<td>2000</td>
</tr>
<tr>
<td>Virtex-4 Block RAM</td>
<td>8</td>
</tr>
<tr>
<td>Global Clock Buffers</td>
<td>2</td>
</tr>
<tr>
<td>Digital Clock Managers (DCM)</td>
<td>1</td>
</tr>
</tbody>
</table>
Configurable PCS Reference Design

- Xilinx CPCS solution can be accessed in application note XAPP759
- Provides a multi-mode soft PCS
  - FC (1G/2G), ESCON/SBCON: Transparent mapping
  - GE: Frame and Transparent mapping
- Dynamically controls PCS mode on each port
  - MGT attributes are partially reconfigured utilizing PPC
  - Clock multiplexing uses local routing
- Scales to multiple ports
  - Each port operates independently with unique clocking
Configurable PCS (CPCS)

- MGT
- High-speed I/Os
- Reference Clocks

CPCS

- 1000BASE-X PCS
- FC PCS
- ESCON PCS

Clock Module

- Control/Status Module
- PPC405

Frame/Transparent Mapped Client Interfaces

Transparent Mapped Client Interfaces

Common Client Interfaces

External Processor Interface
1-GE & 10GE MAC IP Cores

- Only FPGA supplier with UNH proven 1GE & 10GE MAC IP
  - Tested against 802.3 Standards Compliance
  - Interoperability tested with major vendors’ network equipment
- Highly parameterizable
  - Flexibility to optimize GEMAC & 10GEMAC IP cores based on the application needs
- Features well-suited for Ethernet over SONET/SDH application
  - Supports jumbo frame of any size --> Results in efficient payload transport
  - VLAN frame support --> Essential for metro Ethernet applications
  - Cut through operation minimizes latency --> Ideal to meet SONET/SDH protocol latency requirements
- Supports broad range of PHY interfaces

<table>
<thead>
<tr>
<th>1GE</th>
<th>10GE</th>
<th>System Benefit</th>
</tr>
</thead>
<tbody>
<tr>
<td>GMII/RGMII</td>
<td>1000 Base-X</td>
<td>broad range of PHY choices</td>
</tr>
<tr>
<td>1000 BASE-X/SGMII</td>
<td>XAU1</td>
<td>less power &amp; board space</td>
</tr>
<tr>
<td>TBI</td>
<td></td>
<td>Low cost</td>
</tr>
</tbody>
</table>
1 GEMAC with PCS/PMA

<table>
<thead>
<tr>
<th>MAC</th>
<th>PCS/PMA</th>
<th>Slices</th>
</tr>
</thead>
<tbody>
<tr>
<td>1GE</td>
<td>1000 Base-X</td>
<td>1172</td>
</tr>
<tr>
<td>1GE</td>
<td>TBI</td>
<td>1298</td>
</tr>
<tr>
<td>1GE</td>
<td>None</td>
<td>743</td>
</tr>
</tbody>
</table>
10 GEMAC with XAUI Interface

- Optimizable core with right features for EOS applications
- UNH Compliance Tested

<table>
<thead>
<tr>
<th></th>
<th>MAC</th>
<th>PCS/PMA</th>
<th>Slices</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 GE</td>
<td></td>
<td></td>
<td>2331</td>
</tr>
<tr>
<td>XAUI</td>
<td></td>
<td></td>
<td>3366</td>
</tr>
</tbody>
</table>
Embedded Tri-Mode Ethernet MAC in V-4

- Fully Integrated 10/100/1000 Mbps Ethernet Media Access Controller
  - Up to 4 Cores per FX device
  - UNH Compliance Tested
- Use with or without PPC
- Key Benefits
  - 2100 more Slices available for user logic
  - Implement Single-chip 1000 Base-X Ethernet
  - Low cost connectivity due to multiple (MII/GMII/RGMII/SGMII) PHY interfaces support
Fibre Channel Core Highlights

- Auto-negotiable 1Gbps and 2Gbps operation
- Supports all non-loop port types (N, B, E, F)
- Optional 32-bit Statistics counters
- Optional Host Interface
- Supports all classes of FC frames
- Independently configurable TX and RX speeds
- Supports Buffer to Buffer Credit Management and Credit Recovery
- Programmable Timeout values
- User-customizable using CORE Generator
- The only UNH-certified FPGA solution!

<table>
<thead>
<tr>
<th>Speed</th>
<th>Mode</th>
<th>Slices</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 or 2 Gbps</td>
<td>No Host I/F or Statistics</td>
<td>1440</td>
</tr>
<tr>
<td>1 or 2 Gbps</td>
<td>With Host I/F and Statistics</td>
<td>1950</td>
</tr>
</tbody>
</table>
Example Linecard Solution

Virtex-4 FPGA is complimentary to SONET/SDH Framer/Mapper ASSP in the application
Virtex-4 FPGA allows flexible partition which enables customer to implement a low-cost solution.

Example Linecard Solution

- MGT
- MAC/CPCS
- GFP-T
- GFP-F
- VCAT/LCAS
- SONET/SDH Framer
- Optics
- Vitesse VSC911

Virtex-4 FPGA allows flexible partition which enables customer to implement a low-cost solution.
Example Linecard Solution

- Virtex-4 FPGA provides migration path to next generation linecard solution
- Allows customer to leverage legacy devices - leads to faster time-to-market
Ethernet Aggregation (XAPP695)

- SONET framer adaptation
  - 4/8 GE ports to SPI4.2
  - Optional GFP-F (2003)
  - SAR + MUX/DMUX
- Integrated control plane
  - PPC for init/stats/debug
- Reference Design
  - Verilog + EDK + LogiCores
  - Hardware demonstration

- Unique demonstration of PPC control plane
  - Init, stats, debug
Solution Case Study

• Target device - 4VFX60
• Sub-modules in the solution
  — CPCS, MAC, FIFO, GFP, SPI4.2, Misc. logic
• OC-48 solution
  — Four 1g ports
  — Uses only 28% of the slices
  — Smallest device 4VFX20
• OC-192 solution
  — Ten 1g ports or one 10g port
  — Uses 58% of the slices
Xilinx Solutions Address Line Card Designs

**System Interfaces**

- **Integrated Optics**
- **PMD**
- **PHY Layer**
- **Framer/ Mapper/ MAC**
- **Security Processor**
- **Network Processor, Look-up, Classification**
- **Traffic, Queue, Policy Mng.**
- **SerDes + Switch Fabric**
- **Virtex V4**

**FPGA, IP (GbE, POS, HDLC, GFP, RPR)**

1. **Rocket PHY**
2. **CSIX**
3. **PCI, PCI-X**
4. **PCI Express**
5. **Advanced Switching**
6. **Serial RapidIO**
7. **Ethernet**
8. **Proprietary**

**Integrated Optics PMD**

- SFI-4
- XSBI
- SPI-3
- SPI-4.2
- TFI-5
- UTOPIA L2, L3

**Security Processor**

- HyperTransport
- RapidIO
- Proprietary

**Network Processor, Look-up, Classification**

- QDR, QDR-II
- CAM I/F
- RL-DRAM
- DDR-RAM
- FCRAM
- NoBL/ZBT
- Sigma RAM

**Traffic, Queue, Policy Mng.**

- PCI, PCI-X
- PCI Express
- Advanced Switching
- Serial RapidIO
- Ethernet
- Proprietary

**SerDes + Switch Fabric**

- Memory

**Virtex V4**

- **Rocket I/O**
  - Required signaling technology for data plane, control plane and backplane interfacing
  - High-speed I/Os (HSTL, SSTL, GTL, LVDS) - Efficient inter-chip communication
    - Critical for high throughput packet processing
    - PECL for >200MHz clocks
    - Increased bandwidth per I/O enables practical PCB layout
  - High-speed external memory interfaces >200MHz SDR
    - Enables offloading of high performance memory intensive operation
  - High-speed internal Block RAM
    - Maintains linked list headers/packet descriptions

- **DLLs and clock trees**
  - Enables support for multiple clock domains at different clock rates
  - Manages PCB board signal skew

- **High-speed multipliers**
  - Used to calculate packet transmit schedule

- **Power PC** - Efficient implementation of compute intensive algorithms
  - Weighted fair queuing, per flow queuing, security
Reference Slides
GFP Application Example

Support 8 ports programmable to
GFP-T
or
GFP-F

SPI4.2
programmable port address, Store and
forward or cut-through FIFO

Individually
programmable GFP-F
Mapper
(pass-thru GFP-T)

2VP-50
(GFP-F: 8xGE MAC
GFP-T: CPCS)

Intel® IXF19301
Framer/ Mapper w/ GFP-F,
VC and LCAS

Line
OC192

OTN

Intel
OC192
Module

0
1
7 serdes

Programmable World 2004
10 GEMAC Core

- Only FPGA supplier with UNH proven 10 GEMAC IP
  - tested against 802.3ae Standards Compliance & for interoperability with major vendors
  - Eliminates expensive and time consuming interoperability testing for customer equipment
- Enables efficient payload transport with unlimited size jumbo frame support
- VLAN support to enable Metro Ethernet applications
- Implements cut-through operation critical for latency sensitive applications
- Loss-less flow control
- Highly parameterizable
  - Flexibility to optimize 10 GEMAC core based on the application needs
- 10 GEMAC supports both LAN (10.3Gbps) & WAN (OC192 9.953Gbps) Line applications
- Uses 4 embedded RocketIO Transceivers
Seamless Serial Solutions
(622 Mbps to 11.1 Gbps)

* RocketPhy is SONET Compliant. Virtex-4 Supports SONET Payload above 2.5 Gbps.
## Virtex-4 FX Family

<table>
<thead>
<tr>
<th>Logic Cells</th>
<th>4VFX12</th>
<th>4VFX20</th>
<th>4VFX40</th>
<th>4VFX60</th>
<th>4VFX100</th>
<th>4VFX140</th>
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<tbody>
<tr>
<td>BRAM Blocks</td>
<td>12,312</td>
<td>19,224</td>
<td>41,904</td>
<td>56,660</td>
<td>94,696</td>
<td>142,126</td>
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<tr>
<td>Block RAM Kbits</td>
<td>36</td>
<td>68</td>
<td>144</td>
<td>232</td>
<td>376</td>
<td>552</td>
</tr>
<tr>
<td>DCMs</td>
<td>4</td>
<td>4</td>
<td>8</td>
<td>12</td>
<td>12</td>
<td>20</td>
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<tr>
<td>DSP Slices</td>
<td>32</td>
<td>32</td>
<td>48</td>
<td>128</td>
<td>160</td>
<td>192</td>
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<td>System Monitors</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Max Select IO</td>
<td>320</td>
<td>320</td>
<td>448</td>
<td>576</td>
<td>768</td>
<td>896</td>
</tr>
<tr>
<td>Total IO Banks</td>
<td>9</td>
<td>9</td>
<td>11</td>
<td>13</td>
<td>15</td>
<td>17</td>
</tr>
<tr>
<td>Processors</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2</td>
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</tr>
<tr>
<td>EMACs</td>
<td>2</td>
<td>2</td>
<td>4</td>
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<td>RocketIO™ MGTs</td>
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<td>12</td>
<td>16</td>
<td>20</td>
<td>24</td>
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<table>
<thead>
<tr>
<th>Package</th>
<th>Size</th>
<th>MGT</th>
<th>IO</th>
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<tbody>
<tr>
<td>SF363</td>
<td>17</td>
<td>0</td>
<td>240</td>
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<tr>
<td>FF668</td>
<td>27</td>
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<td>FF672</td>
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<td>12</td>
<td>352</td>
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<td>20</td>
<td>576</td>
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<td>FF1517</td>
<td>40</td>
<td>24</td>
<td>768</td>
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<tr>
<td>FF1760</td>
<td>42.5</td>
<td>24</td>
<td>896</td>
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</tbody>
</table>

(Y) X
Y = MGT Channels and X = IO capacity
Xilinx Solution Space

FC SAN

IP SAN

IP LAN

SONET/SDH RING

CPCS

GFP-F/T

SPI-3/4 CORE

Mixed Fibre Channel, Ethernet Links

SONET FRAMER
## Sub-systems of Xilinx Solution

<table>
<thead>
<tr>
<th>Networking IP</th>
<th>Reference Designs</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P$ 10 Gb Ethernet MAC (w/ XAUl option)</td>
<td>Configurable PCS reference design</td>
</tr>
<tr>
<td>$P$ XAUl</td>
<td>Ethernet aggregation reference design (XAPP095)</td>
</tr>
<tr>
<td>$P$ 1 Gb Ethernet PCS/PMA</td>
<td>Intel GFP mapping reference design</td>
</tr>
<tr>
<td>$P$ 10/100/1000 Mb Ethernet MAC</td>
<td>Silicon</td>
</tr>
<tr>
<td>$P$ C 10/100 Mb Ethernet MAC</td>
<td>V2-Pro</td>
</tr>
<tr>
<td>$X$ GigE MAC to SPI-4.2 Bridge</td>
<td>V2-Pro X</td>
</tr>
<tr>
<td>$X$ 10/100 Base-T Bridge Encoder/Decoder</td>
<td>V4</td>
</tr>
<tr>
<td>$P$ SPI-4.2 (POS -PHY L4)</td>
<td></td>
</tr>
<tr>
<td>$P$ SPI-4.2 Ule (reduced area, 1/4 rate)</td>
<td></td>
</tr>
<tr>
<td>$P$ SPI-3 (POS -PHY L3)</td>
<td></td>
</tr>
<tr>
<td>Quad SPI-3 to SPI-4.2 Bridge Ref Des.</td>
<td></td>
</tr>
<tr>
<td>$P$ GFP</td>
<td></td>
</tr>
<tr>
<td>$A$ Framer</td>
<td></td>
</tr>
<tr>
<td>$A$ VCAT7/CAS</td>
<td></td>
</tr>
<tr>
<td>$P$ FiberChannel 1x/2x</td>
<td></td>
</tr>
</tbody>
</table>

$ - License Fee,  $P - Parameterized,  $C - CoreConnect I/F,  $A - Alliance Core
Fibre Channel Core

- Single or Dual-speed core running at 1 Gb (1062.5 Mb), 2 Gb (2125 Mb) or 1 Gb / 2 Gb per second (negotiable).
- Common internal core clock frequency maintained at 53.125 MHz independent of communication rate
- Industry’s first UNH tested programmable solution for interoperability and standards conformance!
Xilinx MPPS Card Solutions

Multi-Rate Line Card

GbE
1G & 2G FC
ESCON

SFP Optical Module

RocketIO Transceiver (PMA)

Configurable PCS

FIFO & Channel Selection

MUX

GFP-F (GbE)

GEP-T (FC, ESCON)

SPI-3

SONET Framer

Ethernet
PPP
FFC
FICON
ESCON
DVB-ASI

GFP-F

GFP-T

SPI-3

SPI-4.2

Sonet (vc/lcas)

Krista M. Marks:
Update figure to be correct: FIFOs come between CPCS and GFP core
# Xilinx Solution Resource Utilization

<table>
<thead>
<tr>
<th>Modules</th>
<th>OC-48 GFP-F solution Slices</th>
<th>OC-48/192 GFP -T solution Slices</th>
</tr>
</thead>
<tbody>
<tr>
<td>10GE w/XAUI</td>
<td></td>
<td>4,430</td>
</tr>
<tr>
<td>Multi-protocol interface (xN)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10/100/1000M embedded MAC</td>
<td>0 (embedded)</td>
<td></td>
</tr>
<tr>
<td>CPICS</td>
<td>4,368</td>
<td>10,920</td>
</tr>
<tr>
<td>GFP -F/T</td>
<td>2,000</td>
<td>5,000</td>
</tr>
<tr>
<td>Aggregation</td>
<td>1250</td>
<td>1250</td>
</tr>
<tr>
<td>CPI</td>
<td>1750</td>
<td>1750</td>
</tr>
<tr>
<td>FIFO</td>
<td>3000</td>
<td>5800</td>
</tr>
<tr>
<td>SPI4.2</td>
<td>3900</td>
<td>3900</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>16,268</strong></td>
<td><strong>33050</strong></td>
</tr>
</tbody>
</table>

Notes: (1) N is the number of CPICS ports implemented in the system. N = 1, 2, ..., 8
(2) Resource utilization depends on settings of CPICS configuration parameters.
GFP-F Only Core Topology

- Xilinx reference design for complete system solution
- Frame buffering
  - Store and forward on a per-channel basis
  - Round robin between N channels
  - Clock adaptation (N client clocks to one system clock)
  - Applicable to both GFP-F and GFP-T
- Utilize on-chip or off-chip RAM
Ethernet/FC Interoperability

- Xilinx IP solutions tested by **UNH Interoperability Lab**
  - 10/100, 1GE, and 10GE MAC
  - FC
  - Tested against IEEE compliance standards
  - Multiple configurations tested, including XAUI

- UNH using Xilinx board for pre-test and pattern generation

- Only FPGA supplier participating
Thank you!