Accelerate High-Performance Real-Time Video & Imaging Applications with FPGA & Programmable DSP
Agenda

• Overview

• FPGA/PDSP HW/SW Development System Platform: TI EVM642 + Xilinx XEVM642-2VP20

• FPGA for Algorithm Acceleration: H.264/AVC SD Video Encoder

• Xilinx MPEG-4 Codec Reference Design

• Xilinx SysGen Co-Sim Design and C/C++
Analysts See Explosive Growth in Digital Media Market

Advanced Codec Unit Shipments (in millions)

Source: In-Stat/MDR, 6/04

Advanced Codecs Include:
- MPEG-4
- H.264
- WMV9
Using FPGAs and DSPs Together for Video Processing

Application examples
- **DSP only**
- **DSP + FPGA**

- **Codecs**
  - H.264
  - MPEG4
  - MPEG2
  - JPEG
  - H.263

- **Coding**
  - Encode
  - Decode
  - Simultaneous encode/decode

- **Channels**
  - Few
  - Many
  - HD
  - SD
  - CIF
  - QCIF
  - D1

- **Resolution**
  - HD
  - SD
  - CIF
  - QCIF
  - D1

**Codec Examples**
- JPEG
- MPEG2
- MPEG4
- H.263
- H.264

**Coding Examples**
- Encode
- Decode
- Simultaneous encode/decode

**Channels Examples**
- Few
- Many
- HD
- SD
- CIF
- QCIF
- D1
Targeted Video Applications

- Real-time 30fps TV/VGA resolution encode & decode
- Integrated audio, video & streaming DSP controller
- Headroom available for High-Def feature enhancements & codec extensions

Features
- 30fps CIF resolution encode & decode
- Integrated audio, video & streaming DSP controller
- Headroom available for feature enhancements & codec extensions

Features
- Real-time 30fps TV/VGA resolution encode & decode
- Integrated audio, video & streaming DSP controller
- Headroom available for High-Def feature enhancements & codec extensions
DSPs and FPGAs: Complementary Solutions

• FPGAs Suitable for Parallel Data-Path Bound Functions/Problems

• SW/HW Co-Design Inner-Loop Rule: “Any C/C++ that requires tight inner-loop assembly codes probably should be in hardware”

• FPGAs typically complement programmable DSPs in high-performance real-time systems in one or more of the following ways:
  – System logic muxing and consolidation
  – New peripheral or bus interface implementation
  – Performance acceleration in the signal processing chain
**TI DSP Architecture**

**Multiple bus architecture**
- Large number of simultaneous inputs and outputs (avoids bottleneck in processing)
- Allows parallel fetching of an instruction and data

**Extensive pipelining**
- Executes parts of several instructions in a single cycle

**Special instructions**
- Combines several operations into a single cycle

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**TMS320C64x™**

**Peripherals**
- Video port-0
- Video port-1
- Video port-2
- 10/100 Ethernet MAC
- 66 MHz PCI
- 64-Bit EMIF

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**L1 Program Cache**

**VelociTI.2™**
- Instruction Fetch
- Instruction Dispatch Packet Boundary Span
- Instruction Decode
- Control Registers
- Advanced Emulation
- Interrupt Control

**Data Path 1**
- Register File A
  - A15-A0
  - A31-A16

**Data Path 2**
- Register File B
  - B15-B0
  - B31-B16

**L1 Data Cache**

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**Courtesy of Texas Instruments**

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FPGAs for High-Performance Co-DSP Applications

FPGA
- Internal Memory
  - BRAM
  - Video Line buffers/deep and wide
  - Cache tag memory/dual port RAM
  - Large FIFOs/packet buffers
- Memory interface
  - SDRAM/DDR

 DSP
- Serial Interfaces
  - Rapid I/O, SR I/O
  - 10GigBit Ethernet
  - HyperTransport
- Internal memory
  - L1/L2 cache memory
  - 256K RAM
  - Configurable cache/RAM
- Memory interface
  - SDRAM
  - 4 CE spaces

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The SX family emphasizes Xilinx commitment to Co-DSP applications by providing a strong skew toward dedicated arithmetic units versus logic.

- **4VSX25**
  - 2,650 CLB
  - 128 BRAM
  - 128 XtremeDSP Slices to augment DSP Math

- **Largest device - 4VSX55**
  - 6,144 CLB
  - 320 BRAM
  - 512 XtremeDSP Slices to augment DSP Math
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Xilinx Daughter Card & TI EVM Board Reference Design

- TI TMS320DM642 EVM Board getting excitement and traction at TI DSP accounts
  - Texas Instruments TMS320DM642 specifically designed for video DSP
    - 720 MHz, 8 instructions per clock, 5.7 GIPS
  - Designed by Spectrum Digital
    - TI’s primary DSP Board and Board Sales Channel
  - Designed to support DSP algorithm development and demonstration for streaming video

- Xilinx Daughter Card to augment DSP Math
  - P20, 88 x 200 MHz = 17 GMACs
  - P50, 232 x 200 MHz = 46 GMACs
  - SX55, 512 x 500 MHz = 256 GMACs
  - High bandwidth, large depth Frame Buffer Memory
FPGA as DSP Accelerator

Xilinx XEVM642-2VP20 daughter card

- V2P20-50 1\textsuperscript{st} G
- V4SX25-55 2\textsuperscript{nd} G
- H.264/AVC SD Codec
- Microsoft WMV-9 (VC-9) SD Codec

Source: Spectrum Digital
TI EVM642 and Xilinx XEVM642-2VP20
XEVM642-2VP20 as a Video DSP Pre-processor

FPGA Pre-processor

XEVM642-2VP20 Board

EVM Interface

TI DM642

EVM Board

To Display
XEVM642-2VP20 as a Video DSP Co-processor
The FPGA consists of two functional blocks that control the arbitration of the DMA Engines of the HDD and the DM642 DSP:

- DM642 EDMA State Machine controls the continuous streaming of Data to/from the EMIF A Peripheral of the DM642 DSP.
- UltraDMA HDD State Machine controls the continuous streaming of Data from the FIFO to/from the HDD Sectors.
Virtex-4 SX/DM642 Cable Box

Statistical-Remultiplexor:
Cable head-end box, residing with the local cable-service provider that
- Takes in multiplexed digital channels
- Incorporates local/targeted advertisements
- Uses FPGAs in Design
- Encodes & inserts local programming content
- Outputs a specific subscriber’s cable package

Satellite
- DVB ASI/DHEI
- 12-18 channels/Transponder

Input/Output Control
- Virtex-4 SX
- 800 Mbps
- Local Bus

Video Processing Units
- Transrating/transcoding
- DM642
- SDRAM
- DM642
- SDRAM
- DM642
- SDRAM

Host I/F Bridge
- Video Buffer
- RISC
- ROM

Ethernet
- 10/100Mbps

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Video Solution Support

- Video DSPs
  - Texas Instruments
- Board & Manufacturing
  - Spectrum Digital, Inc.
- DSP Algorithm Support
  - Ittiam
  - UBVideo
  - W&W Communications (DSP Research)
- Xilinx Expert Design Services
  - Nuvation
- Reference Designs Available
  - H.264/AVC SD Codec (Q1’05)
  - Multi-channel Video PIP + JPEG Web Server (Q4’04)
- Contact Xilinx DSP Marketing for Details
Demo #1
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Applications for H.264/AVC

• Entertainment Video (1 - 8+ Mbps, higher latency)
  – Broadcast / Satellite / Cable / DVD / VoD / FS-VDSL / …

• Conversational H.32X Services (usu. <1Mbps, low latency)
  – H.320 Conversational
  – 3GPP Conversational H.324/M
  – H.323 Conversational Internet/unmanaged/best effort IP/RTP
  – 3GPP Conversational IP/RTP/SIP

• Streaming Services (usu. lower bit rate, higher latency)
  – 3GPP Streaming IP/RTP/RTSP
  – Streaming IP/RTP/RTSP (without TCP fallback)

• Other Services
  – 3GPP Multimedia Messaging Services
H.264/AVC Overview

- Video coding layer is based on hybrid video coding and similar in spirit to other standards but with important differences

- New key features are:
  - Enhanced motion compensation
  - Small blocks for transform coding
  - Improved deblocking filter
  - Enhanced entropy coding

- Bit-rate savings generally 50% or better against any other standard for the same perceptual quality (especially for higher-latency applications allowing B pictures)

- Increased complexity relative to prior standards

- Standard of both ITU-T VCEG and ISO/IEC MPEG

- Standardization completed in May 2003
**H.264 Major Gains**

H.264, MPEG 4 part 10, AVC Acceleration: Combining the Advantages of Hardware and Software

- De-blocking Filter, CAVLC and CABAC Entropy coding
- Enhanced Motion prediction
  - Intra-prediction for I frames using 4X4 blocks
  - Spatial and temporal prediction using multiple block sizes and ¼ pel

Source: Diagram by Nikkei Electronics, based on data released by Sony Computer Entertainment
Strategy and Advantages of FPGA/DSP Combination

Strategy:

• Migrate computationally intensive modules such as Motion estimation, Intra prediction and CABAC to the FPGA
  – DSP orchestrates synchronization of these modules
• The result is a much faster, higher quality and more powerful implementation of H.264

Advantages:

• Move computational intensive modules to FPGA
• Can achieve D1/HD resolution
• Enhances a DSP software only solution with co-processing parallelism
H.264/AVC SD System

Texas Instruments DM642

Video /in

Video /out

Video /in

Video /out

VLC Rate Ctrl Ref Index

SDRAM Shared Memory

Ctrl Registers

flags/ref_ptr/orig_ptr/rec_ptr/ref_index

Arb DMA

Dual-Port RAM Orig/Ref/Rec MV Level/Run Coef 70 KB

Diff

RLC (CAVLC/CABAC)

Xilinx FPGA V2P50

IT/ZZ/Q

Buffer

MV Predict

ME/MC

Intra_Pred

SAD

SAD

SAD

IIT/IZZ/IQ

Buffer

ADD

De-Block Filter

Mode Decision

Buffer

Buffer

Buffer

Buffer

Buffer
Key Modules for Hardware Acceleration

Motion compensation/estimation
- H.264 Motion compensation block size has 8 modes: 16x16, 16x8, 8x16, 8x8, 8x4, 4x8, 4x4 and skip mode
- Previous standards: MPEG 1/2/4, H.263 three modes at most
- SUB-pel MC for H.264 is ¼ pixel

Intra Prediction
- 4x4 blocks are used for luma prediction, and all 9 modes for luma at 4x4
  four modes for chroma 8x8

Entropy Coding
- Two options in H.264: CAVLC (Context Adaptive Variable Length Coding) and CABAC (Context-based Adaptive Binary Arithmetic Coding)
- CABAC utilizes arithmetic coding with probability models as opposed to variable length coding
Complexity of Codec Design

- New design includes relaxation of traditional bounds on complexity (memory & computation) – rough guess 2-3x the MIPS, ROM & RAM requirements of MPEG-2 for decoding, 3-4x for encoding
- Particularly an issue for low-power (e.g. mobile) devices
- Problem areas
  - Smaller block sizes for motion compensation (cache access issues)
  - Longer filters for motion compensation (more memory access)
  - Multi-frame motion compensation (more memory for reference frame storage)
  - In-loop deblocking filter (more processing & memory access)
  - More segmentations of macroblock to choose from (more searching in the encoder)
  - More methods of predicting intra data (more searching)
  - Arithmetic coding (adaptivity, computation on output bits)
Video Industry Roadmap

- MPEG-4 Simple Profile/Advanced Simple Profile
- H.264 – JVT – MPEG-4 Part 10
  - About 40% compression gain over MPEG-2
  - 50% gain with CABAC
  - Likely successor to MPEG-2
  - Quite complex at resolution greater than SIF (D1, HD)
- WMV (aka WMV-9 / VC-9)
  - Between ASP and H.264, closer to ASP (no CABAC)
- HD-DVD initiatives (DVD-Forum)
- Broadcast Infrastructure
  - In the US, High Definition mandated by FCC
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MPEG-4 SP Video Codec

HW on FPGA
SW on DSP
MPEG-4 SP Video Codec

HW on FPGA
SW on Host PC
MPEG-4 SP Codec FPGA HW Place & Route Floor Plan

Encoder

Decoder

FPGA Device: XC2V3000-4; 14336 total slices

- mpeg4 decoder
- memory controller
MPEG-4 SP Codec FPGA HW
Resources & Performance

<table>
<thead>
<tr>
<th>Encoder Hardware Block</th>
<th>memory</th>
<th>bits</th>
<th>BRAMs</th>
<th>Slices</th>
<th>MULTs</th>
<th>ZBT SRAM (bytes)</th>
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<tr>
<td>Capture Controller</td>
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<th>Slices</th>
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<td>Motion Compensation</td>
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<td>Texture/IDCT</td>
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<td>Auxiliary Controllers</td>
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<td>390</td>
<td>0</td>
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<tr>
<td><strong>Total</strong></td>
<td>40</td>
<td>6500</td>
<td>27</td>
</tr>
</tbody>
</table>

- Full SD Enc/Dec Reference Design; Multi-channel decode cap.
- Enc @ ~47,520 MB/s; Dec @ ~190,000 MB/s; Target Clock Rates: 100-133 MHz
- Encoder core is estimated at ~7400+ Slices, 38 Block RAMs, 2 MULTs
- Decoder core is estimated at ~6500 Slices, 40 Block RAMs, 27 MULTs
Demo #2
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Xilinx System Generator

- A complete system design requires high level of abstraction that’s independent of implementation details.
- System level approach enables development and understanding from block diagram perspective.
- Hence, there is a need for high-level design environments to model and simulate mathematical theories, systems, signals, and algorithms.
Simulink to Target Design Flow

System and Algorithm Specification & Partitioning (Floating point)

Subsystem Design (Cycle accurate, bit true)

Code Generation, Verification (HDL, C, ASM)

Simulink Development Environment

Real-Time Workshop

System Generator for DSP

Microcontroller

TI DSP

Xilinx FPGA
MPEG & H.26x C/C++ Reference Software Code

• Provide Shared Memory Architecture
• Provide DLL Library for API Calls from C/C++ Code
• Provide Xilinx Block Sets for Shared Memory in Matlab/Simulink/SysGen
• Example based on Xilinx Own C/C++ Video Codec Software Model
• Replace SW to HW Co-Sim for Motion Estimation Function Block
More Information on the Joint Video Solution

• Register for Xilinx DSP Technical Training
  – Simulink for DSP
  – DSP Design Flow
  – Advanced DSP Implementation Techniques
• Evaluate Xilinx IP cores
• Evaluate System Generator for DSP
  www.xilinx.com/dsp

• Register for Texas Instruments Developers Conference (TIDC)
• Register for Video Seminars
  www.ti.com/videoseminars
• Download App notes:
  EMIF interface
  LVDS High-Speed AD Converter
  www.ti.com/dm64xpr
Thank You
XEVM642-2VP20 I/O Expansion

I/O Expansion Using Cable Between Two Cards
I/O Expansion Using Top and Bottom EVM Connector Between Two Cards
XEVM642-4VSX25 I/O and TI DSP Expansion

TI EVM642 Board

Xilinx XEVM642-4VSX25 or TI I/O Expansion Card(s)
High-Performance Real-Time Video & Imaging Applications

• Professional Audio/Video Broadcast Encoders and Head-end Equipments (i.e. Tandberg TV, Motorola, Scientific Atlanta, Thomson)

• Professional Digital Video Editing Equipments (i.e. Avid, Matrox)

• Professional Audio/Video Test Equipments (i.e. Tektronix, Agilent)

• Professional Digital Video Cameras and Recorders (i.e. Sony, Panasonic)

• Audio/Video Teleconferencing Systems (i.e. Polycom, Sony, Tandberg TV)

• High-Quality Video Surveillance & CCTV Systems (i.e. Pelco, Axis)
Xilinx 2VP20/TI DM642 PIP Reference Design

- 2VP20 DaughterCard
  - De-interlacing
  - Resizing
  - Merging PIP
  - Interlacing
  - Back to DM642
  - Video signal over Ethernet
- Available for Free Download