Programmable Logic
• So far, have only talked about PALs (see 22V10 figure next page).
• What is the next step in the evolution of PLDs?
  – More gates!
• How do we get more gates? We could put several PALs on one chip and put an interconnection matrix between them!!
  – This is called a Complex PLD (CPLD).
Any other approaches?
Another approach to building a “better” PLD is place a lot of primitive gates on a die, and then place programmable interconnect between them.

Field Programmable Gate Arrays
The FPGA approach to arrange primitive logic elements (logic cells) arrange in rows/columns with programmable routing between them.

What constitutes a primitive logic element? Lots of different choices can be made! Primitive element must be classified as a “complete logic family”.

• A primitive gate like a NAND gate
• A 2/1 mux (this happens to be a complete logic family)
• A Lookup table (i.e., 16x1 lookup table can implement any 4 input logic function).

Often combine one of the above with a DFF to form the primitive logic element.

Other FPGA features
• Besides primitive logic elements and programmable routing, some FPGA families add other features
• Embedded memory
  – Many hardware applications need memory for data storage. Many FPGAs include blocks of RAM for this purpose
• Dedicated logic for carry generation, or other arithmetic functions
• Phase locked loops for clock synchronization, division, multiplication.
### Altera Flex 10K FPGA Family

#### Table 1. FLEX 10K Device Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>EPP10K10</th>
<th>EPP10K20</th>
<th>EPP10K30</th>
<th>EPP10K40</th>
<th>EPP10K50</th>
<th>EPP10K60</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical gates (logic and RAM)</td>
<td>10,000</td>
<td>20,000</td>
<td>30,000</td>
<td>40,000</td>
<td>50,000</td>
<td></td>
</tr>
<tr>
<td>Note (1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Usable gates</td>
<td>7,000 to</td>
<td>15,000 to</td>
<td>22,000 to</td>
<td>29,000 to</td>
<td>36,000 to</td>
<td>43,000 to</td>
</tr>
<tr>
<td></td>
<td>31,000</td>
<td>50,000</td>
<td>69,000</td>
<td>89,000</td>
<td>118,000</td>
<td></td>
</tr>
<tr>
<td>Logical elements (LEs)</td>
<td>616</td>
<td>1,152</td>
<td>1,728</td>
<td>2,304</td>
<td>2,880</td>
<td></td>
</tr>
<tr>
<td>Logical array blocks (LABs)</td>
<td>72</td>
<td>144</td>
<td>216</td>
<td>288</td>
<td>360</td>
<td></td>
</tr>
<tr>
<td>Embedded array blocks (EABs)</td>
<td>3</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>Total RAM bits</td>
<td>6,144</td>
<td>12,288</td>
<td>12,288</td>
<td>16,384</td>
<td>20,480</td>
<td></td>
</tr>
<tr>
<td>Maximum user I/O pins</td>
<td>134</td>
<td>168</td>
<td>246</td>
<td>314</td>
<td>380</td>
<td></td>
</tr>
</tbody>
</table>

#### Altera Flex 10K FPGA Family (cont)

#### Table 2. FLEX 10K Device Features (cont)

<table>
<thead>
<tr>
<th>Feature</th>
<th>EPP10K70</th>
<th>EPP10K80</th>
<th>EPP10K110</th>
<th>EPP10K120</th>
<th>EPP10K130</th>
<th>EPP10K140</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical gates (logic and RAM)</td>
<td>75,000</td>
<td>105,000</td>
<td>130,000</td>
<td>200,000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Note (1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Usable gates</td>
<td>46,000 to</td>
<td>62,000 to</td>
<td>82,000 to</td>
<td>122,000 to</td>
<td>122,000 to</td>
<td></td>
</tr>
<tr>
<td></td>
<td>118,000</td>
<td>158,000</td>
<td>211,000</td>
<td>314,000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LABs</td>
<td>496</td>
<td>824</td>
<td>852</td>
<td>1,528</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LABs</td>
<td>9</td>
<td>12</td>
<td>16</td>
<td>20</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total RAM bits</td>
<td>10,432</td>
<td>24,576</td>
<td>33,700</td>
<td>42,908</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum user I/O pins</td>
<td>106</td>
<td>406</td>
<td>475</td>
<td>475</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note to table:
(1) For designs that require I/O boundary switching, the total # of I/O locations contributes up to 50,000 additional gates.

### Dedicated memory

![Dedicated memory diagram]
Embedded Array Block

- Memory block, Can be configured:
  - 256 x 8, 512 x 4, 1024 x 2, 2048 x 1
Issues in FPGA Technologies

- Complexity of Logic Element
  - How many inputs/outputs for the logic element?
  - Does the basic logic element contain a FF? What type?

- Interconnect
  - How fast is it? Does it offer ‘high speed’ paths that cross the chip? How many of these?
  - Can I have on-chip tri-state busses?
  - How routable is the design? If 95% of the logic elements are used, can I route the design?
    - More routing means more routability, but less room for logic elements

Issues in FPGA Technologies (cont)

- Macro elements
  - Are there SRAM blocks? Is the SRAM dual ported?
  - Is there fast adder support (i.e. fast carry chains?)
  - Is there fast logic support (i.e. cascade chains)
  - What other types of macro blocks are available (fast decoders? register files?)

- Clock support
  - How many global clocks can I have?
  - Are there any on-chip Phase Logic Loops (PLLs) or Delay Locked Loops (DLLs) for clock synchronization, clock multiplication?

Issues in FPGA Technologies (cont)

- What type of IO support do I have?
  - TTL, CMOS are a given
  - Support for mixed 5V, 3.3V IOs?
    - 3.3V internal, but 5V tolerant inputs?
  - Support for new low voltage signaling standards?
    - GTL+, GTL (Gunning Transceiver Logic) - used on Pentium II
    - HSTL - High Speed Transceiver Logic
    - SSTL - Stub Series-Terminate Logic
    - USB - IO used for Universal Serial Bus (differential signaling)
    - AGP - IO used for Advanced Graphics Port
  - Maximum number of IO? Package types?
    - Ball Grid Array (BGA) for high density IO
Altera FPGA Family Summaries

- Altera Flex10K/10KE
  - LEs (Logic elements) have 4-input LUTS (look-up tables) +1 FF
  - Fast Carry Chain between LE’s, Cascade chain for logic operations
  - Large blocks of SRAM available as well
- Altera Max7000/Max7000A
  - EEPROM based, very fast (Tpd = 7.5 ns)
  - Basically a PLD architecture with programmable interconnect.
  - Max 7000A family is 3.3 v

Xilinx FPGA Family Summaries

- Virtex Family
  - SRAM Based
  - Largest device has 1M gates
  - Configurable Logic Blocks (CLBs) have two 4-input LUTS, 2 DFFs
  - Four onboard Delay Locked Loops (DLLs) for clock synchronization
  - Dedicated RAM blocks (LUTs can also function as RAM).
  - Fast Carry Logic
- XC4000 Family
  - Previous version of Virtex
  - No DLLs, No dedicated RAM blocks

Actel FPGA Family Summaries

- MXDS Family
  - Fine grain Logic Elements that contain Mux logic + DFF
  - Embedded Dual Port SRAM
  - One Time Programmable (OTP) - means that no configuration loading on powerup, no external serial ROM
  - AntiFuse technology for programming (AntiFuse means that you program the fuse to make the connection).
  - Fast (Tpd = 7.5 ns)
  - Low density compared to Altera, Xilinx - maximum number of gates is 36,000
Cypress CPLDs

- Ultra37000 Family
  - 32 to 512 Macrocells
  - Fast (Tpd 5 to 10ns depending on number of macrocells)
  - Very good routing resources for a CPLD