Bilinear Filtering – Part #3

- Start with the datapath used for Part #1
- Add one pipeline stage to the multiplier, and produce a solution
  - This is not as good as having two separate multipliers because you can only launch one new multiplication each clock cycle instead of two
  - However, the clock period will definitely improve.
  - You will have to modify the order in which calculations are performed to take advantage of the pipelined multiplier, and you will have to add more registers to the datapath
- Other notes
  - Single SRAM is still a constraint
  - Interface does not change
  - Cannot use more than 16 states in FSM
  - Total computation for 8 Tnew values must be less than 90 clocks
  - Register-to-register delay must exceed 20 Mhz (use 10K20RC240-3 device from Flex 10K family), use 'Fast' synthesis option
  - 3rd part is worth 200 pts
  - CANNOT chain operators

Testing

- Can use the same testbench from Part #1 or Part #2 to test your design.
- In your report, compare the *time* it takes to compute the 8 T_{new} values for your solution to Part #1 to this solution
  - Remember that time = #clocks * clock_period
- Also compare the number of Logic Cells (LCs) used for part #1 versus part #3 (look at the report files, *.rpt).
- Extra Credit (10 points on any test grade)
  - Register to Register delay must exceed 32 Mhz (CLOSE DOES NOT COUNT)
  - Total computation for 8 Tnew values must be less than 75 clocks