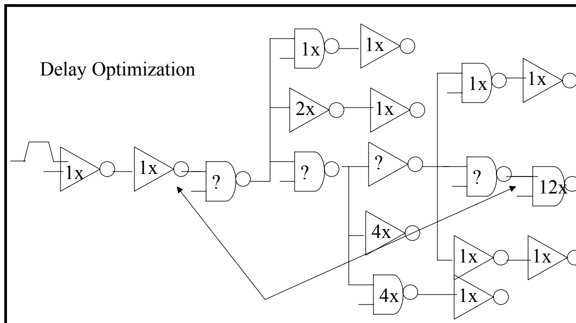
Delay Optimization Homework

- All Spice problems in this homework are to be done for technologies and conditions
  - Tsmc 0.18u technology, Vdd = 2.5 V.
  - AMI 0.5u technology, Vdd = 3.3 V.
  - all input waveforms should have rise/fall times of 200 ps.

Delay Optimization



Size the gates marked with ‘?’ to minimize the delay between the points indicated. Any gates with known gate sizes are FIXED sizes and cannot be changed.

Details

- If the last digit of your student ID modulo 4 is:
  - 0, use 1.4/1 for your 1X inverter, 0.18 TSMC technology
  - 1, use 2/1 for your 1X inverter, 0.18 TSMC technology
  - 2, use 1.4/1 for your 1X inverter, 0.5 AMI technology
  - 3, use 2/1 for your 1X inverter, 0.5 AMI technology
- Scale your 2-input NAND based upon your 1X inverter
  - In your spice model, be sure to use geometry parameters calculated from L,W as discussed in the Spectre example
- When optimizing the delay, optimize only for TPHL
  - will assume that TPLH will be ok
  - this should reduce the simulation workload
- Assume that you only have gate sizes of 1x to 6x available in 0.5x steps.

Part #1: Tilos Optimization

- Use the Tilos algorithm to optimize the gate sizes in 0.5X steps.
  - Increase gate sizes by 0.5X during simulation
- All the gates marked with ‘?’ are available for sizing.
- Once the final gate sizes have been chosen, record both TPLH and TPHL through the optimized path.

Part #2: Logical Effort Optimization

- Use the logical effort approach to optimize the path
  - You will need to use transistor widths to represent load since different gates are being used
- Measure tau, Pinv as specified via Method #2 (see notes) for a 1X inverter.
- Instead of using a computed ‘g’ value for the *nand2*, measure the ‘g’ value for a *nand2* as specified in the notes.
- Also measure *Pnand2* for a 1X sized nand2.
- Use these parameters to optimize the gate sizes
  - The off path loads are fixed, so you will have to chose the gate sizes via iteration
  - Convert the final sizes that you get into the nearest .5X gate size (I do not want to see a gate size specified as 2.68X - round to the nearest 0.5X, or 2.5X in this case.
- Measure both TPLH, TPHL once the gate sizes have been chosen.

Report

- Compare the resulting path delays, gate sizes as optimized in Parts #1, Parts #2
  - Comment upon your results
  - Measure the total power consumed by your circuit for both cases.
- Document all of your calculations/measurements as carefully as possible and present the data in a professional manner