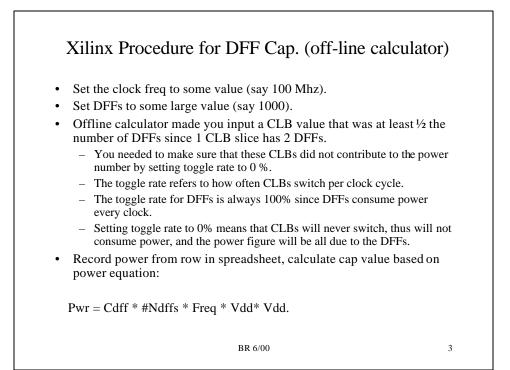
Summary:	Xilinx (low_route	off-line calc,300E) med_route	Altera (300E)
LUT4	.97 pf	1.5 pf	1.2 pf
DFF	.185 pf (re	oute N/A)	.140 pf
	W / CLB, or	about 6uW per LU	JT4.
Spreadshee	t results wer	about 6uW per LU	
about 24 uV Spreadshee	t results wer	1	

Mistakes				
• Xilinx CLB slice = 2 LUT4s, needed to account for this				
• Do not USE total power figure for Xilinx, this included static power disspation				
• Altera included clock tree capacitance as a fixed value for particular die (Same for 200E, 300E; increased for 600E, 1000E because of larger die)				
 When Clock Frequency = nonzero, resulted in non-zero power. If you set toggle freqency to zero, this power did not change as the CLBs were changed, only changed with frequency. This meant it was the clock tree power. 				
 Had to SUBTRACT this power number from the LE power number before calculating LE Capacitance, else got too high a value of LE capacitance. 				
 Clock tree cap = 510 pf for 200E,300E; 825 pf for 600E,1000E. 				
 Xilinx 'cheated' by distributing its clock tree cap (a fixed value per die) among the DFFs. That is why Xilinx DFF cap higher than Altera. 				
BR 6/00	2			



<text><list-item><list-item><list-item><text><text><text><text>

Altera Procedure LUT4s, DFFs

- The procedure for Altera was the same except that that the spreadsheet power included the clock tree power (varied only with clock frequency).
- You could see this contribution by setting the LEs to some non-zero value (say 1000), Frequency to some value (100 Mhz), and DFFs to zero, and Toggle Rate to 0.
 - In the Xilinx spreadsheet, this would give a 0 power value because toggle value is 0% and there are no DFFs.
 - In the Altera spreadsheet, this gives a power figure.
 - If you change the # of LEs, the power figure remained constant. In fact, you could set the # of LEs to 0! This power figure only varied with clock frequency, so it MUST be the clock tree.
- When calculating the DFF, LE cap values, you had to subtract off this constant power due to the clock tree before computing the capacitance figure.

BR 6/00

5