This Course

- You are assumed to be familiar with RTL-level VHDL for synthesis (I.e, ECE 4743/6743)
- This course is intended to cover more advanced features of VHDL useful for system level modeling
  - By system level modeling, I mean non-synthesizeable VHDL code (I.e., an ethernet protocol simulation or bus protocol simulation).
- We will also do a quick overview of Verilog, and concentrate on aspects of Verilog that are not available in VHDL
  - Transistor level modeling in Verilog
- Will also cover advanced synthesis concepts (high-level synthesis) as represented by the Behavioral Compiler tool from Synopsys
- Finally, will look at mixed-mode simulation (combining analog system simulation with digital system simulation).

Tool Usage

- Modelsim (used for both Verilog and VHDL simulation)
- Synopsys Behavioral Compiler (used for high-level synthesis)
- Still investigating options for mixed-mode simulation
- Class WWW page at:

  http://www.ece.msstate.edu/~reese/EE8993

Assignments

- All assignments will be simulation based, 1 or 2 weeks in length
- No assignments will be group based, all individual effort
- No class project
- Will add more simulations than what is currently shown on WWW page.
- No reports are required, just code – assignments will be graded mostly on a pass/fail basis
  - If your code does not work, then do not expect an 'A' or 'B' grade for the assignment – some partial credit will be given but not above the 'C' level
- Academic dishonesty will be dealt with extremely harshly – expect an 'F' grade for the course on first offense.
- I do not accept late assignments because I don't have time to deal with the extra hassle this presents – either turn in your assignment on time or don't bother.

Teaching Style

- I teach VHDL modeling via code examples
  - I cover aspects of the language in the context of complete code examples
  - I DO NOT go page-by-page through the language reference manual (LRM)
- I will announce ahead of time which code examples we will be following – you should print out the COMPLETE VHDL code for the examples as well as the online notes
  - The online notes will have code 'snippets' but will not be able to show the complete files.
  - You need to have the complete VHDL code in front of you so that you can see the context

Grading Policy

The grading policy will be:

- •50% simulations
- •40% Tests (3 tests)
- •10% Final

The class EMAIL list will be the one provided by Information Technology Services (ITS). The email list is

    ece8990-02.spring2002@courses.msstate.edu