Routing Results For:
Silicore SLC1657 Evaluation Board for Altera FLEX 10KE FPGA

August 24, 2001

Test conditions:

Project: CALCDEMO
Device: Altera: epf10k50eqc208-3
Synthesis tool: Altium Accolade PeakFPGA 5.30a
Router: Altera MAX+PLUS II

For more information, please refer to the SLC1657 Technical Reference Manual.

Timing Results (as reported by router):

Timing constraint (MIN): 5.000 MHz (MIPS)
Actual speed (MAX): 7.830 MHz (MIPS)

Device Utilization Results (as reported by router):

<table>
<thead>
<tr>
<th>Chip/Device</th>
<th>Input Pins</th>
<th>Output Pins</th>
<th>Bidir Pins</th>
<th>Memory Bits % Utilized</th>
<th>Memory LCs</th>
<th>Logic LCs % Utilized</th>
</tr>
</thead>
<tbody>
<tr>
<td>AF10EVAL epf10k50eqc208-3</td>
<td>7</td>
<td>4</td>
<td>24</td>
<td>62 %</td>
<td>574</td>
<td>19 %</td>
</tr>
</tbody>
</table>