Features and Benefits

- Implement custom 8051 designs in an Actel ProASICPLUS FPGA using Actel Libero Development Environment Software and QuickCores QC8051 Real-Time Development Kit
- Compatible with Keil Software µVision2 debugger and C compiler
- Includes QuickCores small memory model (2K program reach) synthesizable QC8051 netlist library (compatible with Libero)
- Includes BoxView*** real-time "C" language debugger for QuickCores QC8051
- Includes target board with Actel APA-300 installed
- Flash-USB+ APA Device Programmer/Debugger (included in kit)
  - Programs the Actel APA device
  - JTAG boundary scan controller (SAMPLE/PRELOAD monitoring)
  - JTAG real-time monitor/debugger interface
- 256KB (150ns) external flash memory for program/data storage
- 2-line X 16 character LCD
- 4 user buttons & 8 user LEDs
- RS-232 interface for user applications
- QuickCores QC8051 features:
  - Pipeline architecture allows most instructions execute in a single clock cycle
  - Customizable user SFR block
  - Real-time monitor architecture allows monitoring of internal operations without the use of embedded software routines via JTAG connection
  - Debug logic includes 128-sample deep X 144-channel real-time trace buffer
  - Traces 36-bit time stamp, PC, Instruction Register, PSW, SP, ACC, B, DP, Data RD address/data, Data WR address/data, interrupt acknowledge
  - Unlimited software breakpoints
  - Up to three hardware breakpoints

General Description

When used with Actel Libero integrated design environment software, QuickCores FPGA-8051 Real-Time Development Kit allows you to quickly create and debug custom 8051 designs in an Actel ProASICPLUS FPGA. The kit includes QuickCores small memory model QC8051 softcore, BoxView C language debugger which is compatible Keil Software 8051 C compiler and µVision2 IDE, target board and power supply. Example top-level 8051 references design programming files are also included. Large memory model QC8051 netlist library is available under a separate license.

www.quickcores.com
**QC8051 CPU Module Signal Descriptions** (instantiated at top level of your design)

<table>
<thead>
<tr>
<th>Name</th>
<th>Dir</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PROG_DIN[7:0]</td>
<td>I</td>
<td>QC8051 program instruction bus input</td>
</tr>
<tr>
<td>PROG_DOUT[7:0]</td>
<td>O</td>
<td>QC8051 program write bus used by real-time monitor program write cycles</td>
</tr>
<tr>
<td>PROG_WR</td>
<td>O</td>
<td>Indicates program write during real-time monitor program write cycles</td>
</tr>
<tr>
<td>XDBUS_IN[7:0]</td>
<td>I</td>
<td>QC8051 external data bus input</td>
</tr>
<tr>
<td>XDBUS_OUT[7:0]</td>
<td>O</td>
<td>QC8051 external data bus output</td>
</tr>
<tr>
<td>PCE_n</td>
<td>O</td>
<td>Active low external program memory chip enable</td>
</tr>
<tr>
<td>DCE_n</td>
<td>O</td>
<td>Active low external data memory chip enable</td>
</tr>
<tr>
<td>OE_n</td>
<td>O</td>
<td>Active low external program/data output enable</td>
</tr>
<tr>
<td>WR_n</td>
<td>O</td>
<td>Active low external program/data write enable</td>
</tr>
<tr>
<td>USR_RD_ADDR[7:0]</td>
<td>O</td>
<td>User SFR read address</td>
</tr>
<tr>
<td>USR_WR_ADDR[7:0]</td>
<td>O</td>
<td>User SFR write address</td>
</tr>
<tr>
<td>USR_RD_DATA[7:0]</td>
<td>I</td>
<td>User SFR read data bus</td>
</tr>
<tr>
<td>USR_WR_DATA[7:0]</td>
<td>O</td>
<td>User SFR write data bus</td>
</tr>
<tr>
<td>DIRECT_WR</td>
<td>O</td>
<td>1 = internal data memory “direct” write cycle</td>
</tr>
<tr>
<td>DIRECT_RD</td>
<td>O</td>
<td>1 = internal data memory “direct” read cycle</td>
</tr>
<tr>
<td>MONITOR_DIR</td>
<td>O</td>
<td>1 = internal monitor data memory direct read cycle</td>
</tr>
<tr>
<td>WR_EN</td>
<td>O</td>
<td>1 = internal data memory write enable</td>
</tr>
<tr>
<td>Clock_In</td>
<td>I</td>
<td>External clock input</td>
</tr>
<tr>
<td>CPUClock</td>
<td>O</td>
<td>CPU clock output</td>
</tr>
<tr>
<td>MODE</td>
<td>I</td>
<td>1 = CPU clock = Clock_In / 1; 0 = CPU clock = Clock_In / 4 (use this for external interfacing)</td>
</tr>
<tr>
<td>OP_FETCH</td>
<td>O</td>
<td>1 = opcode fetch cycle</td>
</tr>
<tr>
<td>RMW</td>
<td>O</td>
<td>1 = read-modify-write cycle</td>
</tr>
<tr>
<td>IACK</td>
<td>O</td>
<td>1 = interrupt acknowledge cycle</td>
</tr>
<tr>
<td>INT_REQ</td>
<td>I</td>
<td>1 = interrupt request</td>
</tr>
<tr>
<td>VECTOR[2:0]</td>
<td>I</td>
<td>Bits [5:3] of the interrupt vector loaded into the program counter</td>
</tr>
<tr>
<td>RESET_IN</td>
<td>I</td>
<td>1 = reset</td>
</tr>
<tr>
<td>RESET_OUT</td>
<td>O</td>
<td>1 = reset; this signal internally gated by JTAG debug module</td>
</tr>
<tr>
<td>MONITOR_CYCL</td>
<td>O</td>
<td>1 = monitor cycle</td>
</tr>
<tr>
<td>XDATA_CYCL</td>
<td>O</td>
<td>1 = MOVX instruction; used by memory expansion circuit</td>
</tr>
<tr>
<td>TCK</td>
<td>I</td>
<td>JTAG TCK input</td>
</tr>
<tr>
<td>TDI</td>
<td>I</td>
<td>JTAG TDI input</td>
</tr>
<tr>
<td>TMS</td>
<td>I</td>
<td>JTAG TMS input</td>
</tr>
<tr>
<td>TRST_n</td>
<td>I</td>
<td>JTAG TRST_n input</td>
</tr>
<tr>
<td>TDO</td>
<td>O</td>
<td>JTAG TDO output</td>
</tr>
</tbody>
</table>
FPGA-8051 Real-Time Development Kit
For Actel ProASIC® Plus FPGAs

FPGA-8051 Real-Time Development Kit Netlist Library Top-Level Instantiation Symbols

User-Definable SFR Block

Q8051 CPU (2K Memory Model)

User-Definable Special Function Register Block Symbols Included in FPGA-8051 Netlist Library

DAC7512 Serial Controller Port

Interrupt Controller Block

Dual 16-Bit Counter/ Timer Module

Note: Other modules not shown include general purpose parallel port and external program / data memory extended address banking module. Large Memory Model Q8051 CPU and serial port available under separate license.
QuickCores APA-208 Target Board

ProASICPLUS APA208 Target Board Description

The QuickCores FPGA-8051 Real-Time Development Kit for Actel ProASICPLUS FPGAs includes the APA208 Target Board pictured above. Programming the flash-based ProASICPLUS device is through the FlashUSB+ programming/debug pod included in the kit. Once the device is programmed with the desired QC8051 design, the implemented QC8051 design user application software can be programmed and debugged using the same FlashUSB+ pod. JTAG boundary scan (SAMPLE/PRELOAD) monitoring of the ProASICPLUS APA device pins is also by way of the FlashUSB+ pod interface.

Provided on the APA208 Target Board for your use are 128 Kbytes (x16 bits) external flash memory, 2-line X 16-character LCD, four user buttons and 12.288 MHz oscillator. Although the QuickCores QC8051 Real-Time Development Kit includes an Actel APA-300 ProASICPLUS FPGA, small (2k-reach) memory model QC8051 netlist library which you can use to create your own designs, the APA208 Target Board is shipped with a large memory model QC8051 programmed into the ProASICPLUS APA device and on CD.
BoxView C Language Real-Time Debugger

- Built-in STAPL player programs the target APA device via QuickCores Flash-232+ or Flash-USB+ pod.
- Real-time trace buffer displays 36-bit time stamp, ACC, B, DP, PSW, SP, Data RD address and data, Data WR address and data, PC and Instruction Register contents
- Supports concurrent and remote monitoring and debugging of multiple CPUs
- “Symbols” window allows you to quickly set breakpoints, disassemble, or watch
- Multiple memory windows for data, code, indirect, or external locations
- Graphic display of any memory region allows animation in real-time mode
- On-the-fly monitoring and editing of registers and memory
- Robust JTAG command and scripting language with data logging for automated testing

www.quickcores.com
FPGA-8051 Debug Module 128 Sample X 144-Channel Real-Time Trace Buffer

Disassembly
Instruction Register (IR) contents
Program Counter (aligned with IR)
Interrupt Acknowledge (“+”)
Internal Data Write data
Internal Data Write address
Internal Data Read data
Internal Data Read address
Stack Pointer (SP)
Program Status Word (PSW)
Data Pointer (DP)
B Register (B)
Accumulator (ACC)
36-bit time stamp
Keil Software µVision2 IDE Key Points

- Provided with the FPGA-8051 Real-Time Development Kit are the appropriate .dlls which will allow seamless operation with Keil Software µVision2 IDE and C51 compiler.
- Concurrent real-time monitoring and debug of multiple CPUs is supported when µVision2 IDE is used in combination with Domain Technologies BoxServer and BoxView Debugger.
- The FPGA-8051 real-time trace buffer is supported under µVision2 “Peripherals” menu item.
FPGA-8051 Real-Time Development Kit for ProASICPLUS Contents

The FPGA-8051 Real-Time Development Kit for ProASICPLUS comes with the following items:

- QuickCores APA-208 target board with APA-300 ProASICPLUS FPGA installed and preprogrammed with large memory model QuickCores FPGA-8051 microcontroller
- BoxView real-time C language debugger with integral STAPL player device programmer/driver
- QuickCores small (2k program reach) memory model netlist library targeted Actel ProASICPLUS FPGAs and restricted for use with Libero
- Flash-USB+ APA device programmer/debug pod
- 9-volt power supply
- Target board schematics
- User Guide
- Example large memory model FPGA-8051 top-level and user SFR designs in Verilog and compiled .rpd file format
- Required dlls for use with Keil Software μVision2 IDE

QuickCores Design Services

Along with its microcontroller IP, QuickCores also offers non-recurring engineering (NRE) design services to assist customers with integrating QuickCores microcontroller IP into their designs. This service is available on a quotation basis. Other services include development of custom application software, both on the host PC side and on the target embedded application side.

Ordering Information

FPGA-8051 Real-Time Development Kit part number (small memory model): QC8051-RTDK-APA-S

Contact Information:

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Tel: (972) 578 1121
Fax: (972) 578 1086
Email: sales@quickcores.com

Discount Coupon

Purchase a QuickCores QC8051 Real-time Development Kit (small memory model) before December 1, 2003 and receive 25% off the list price of $595.

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