

INTEGRATED CIRCUITS

---

**DATA SHEET**

I2C TRANSMITTER/RECEIVER

---

PRODUCT SPECIFICATION

2002. Nov 28

# 1. Claims and assumptions (Features and characteristics)

## 1.1 General Information

### 1.1.1 IP

Soft IP

### 1.1.2

I<sup>2</sup>C BUS    BUS    Device    2    bi\_direction serial  
 Bus(serial clock : SCL, serial data SDA)    .    Device  
 Address 가    ,    가    .  
 Master    clock signal    Bus    Data  
 Device    Device    Slave    .

I<sup>2</sup>C Bus    Data    Start condition    Stop condition  
 , SDA    Data    Clock    high period    stable    .    SCL    low  
 data line    가 high    low    .    Start condition    SCL    high  
       SDA    가 high-to-low    ,    Stop condition    SCL  
 low    SDA    가 low-to-high    .

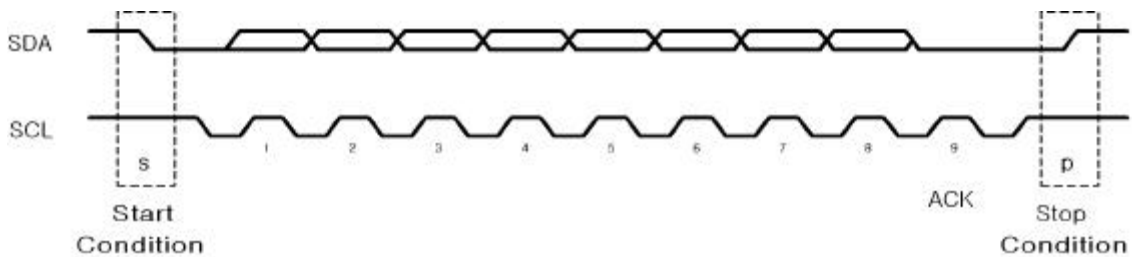
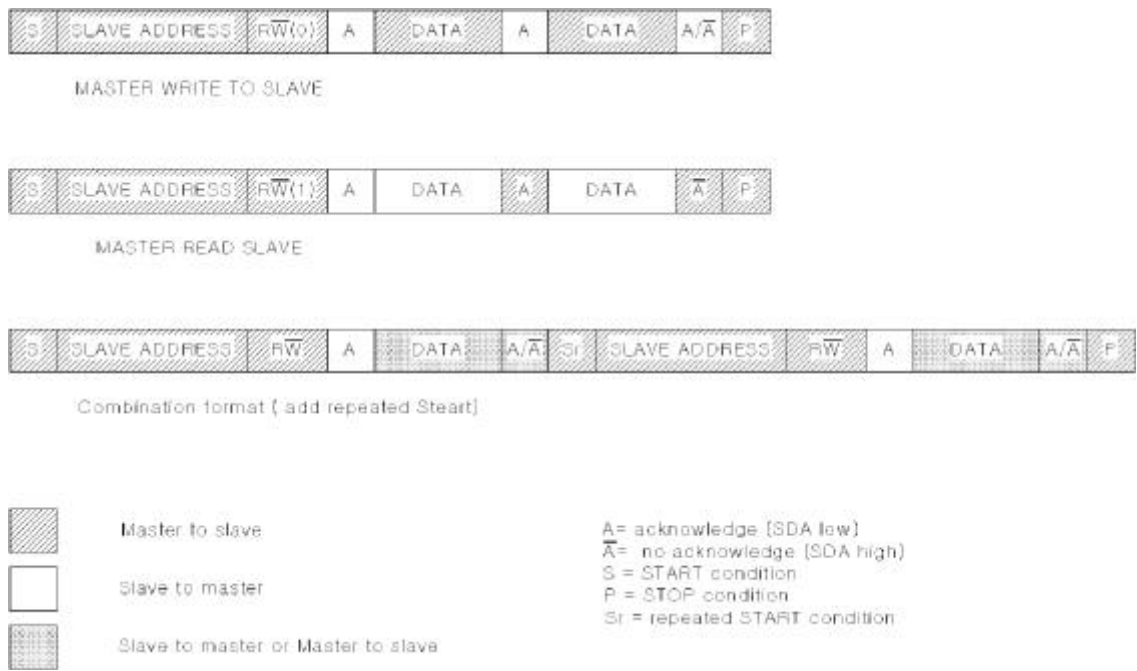


Figure 3 Data transfer on I<sup>2</sup>C Bus

data packet    9clock    8bit    dta    1bit    acknowledge bit  
 Master    Slave    start, slave address, data transfer, stop 4

I<sup>2</sup>C protocol    7bit and 10bit addressing    IP    7bit addressing mode

Start condition    slave\_address    , address    7bit    R/W\_bit가  
       R/W = '1'    request data(read)    R/W = '0'    data  
 transmission(write)    .    slave가 master    address    9  
 clock    SDA\_Bus '0'    acknowledge signal    ,  
 R/W\_bit    byte    data    , master  
 stop    .    master가 stop condition    start condition  
 repeat start    .



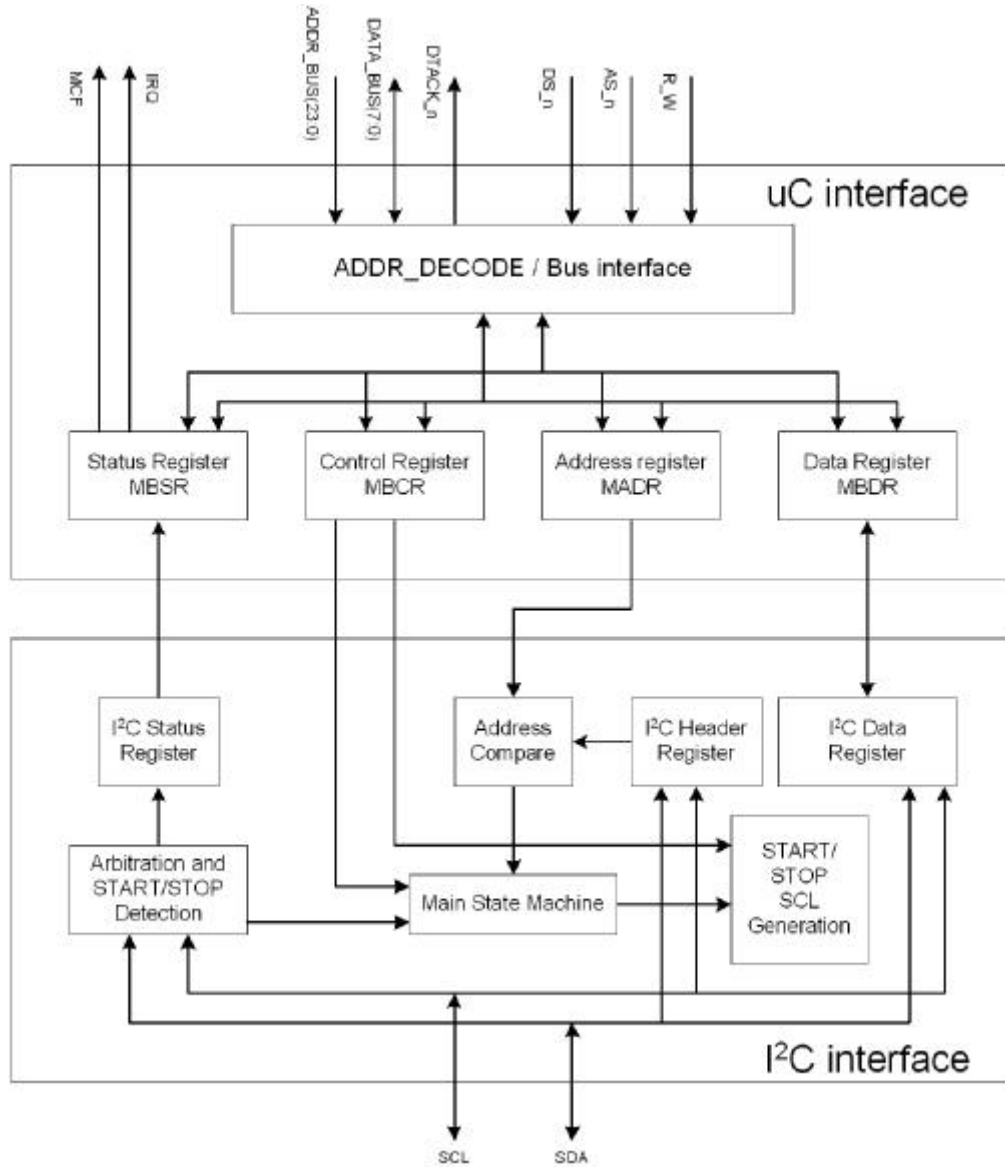
**Figure 2 Data transfer format on I2C Bus**

1.13

2. Verification of claims and assumptions (Reference environment)

### 3. Block Diagram

Figure 3 Data transfer format on I<sup>2</sup>C Bus



### 4. I<sup>2</sup>C Bus Controller Register Description

Table 1 : Address Register (MADR : \$8Dh)

Bit Location	Name	μ C Access	Description
7-1	Slave address	Read/ Write	Slave mode I <sup>2</sup> C controller
0	-	-	

**Table 3 : Control Register (MBCR : \$91h)**

Bit Location	Name	$\mu$ C Access	Description
7	MEN	Read/Write	I <sup>2</sup> C Controller Enable.
6	MIEN	Read/Write	Interrupt Enable
5	MSTA	Read/Write	Master/Slave Mode Select "0"->"1" : master mode Start condition "1"->"0" : slave mode Stop condition 가 Stop condition
4	MTX	Read/Write	Transmit/Receive Mode Select "1" : I <sup>2</sup> C master "0" : I <sup>2</sup> C master
3	TXAK	Read/Write	Transmit Acknowledge Enable "1" : ACK bit = "1" no ack. "0" : ACK bit = "0" ack.
2	RSTA	Read/Write	Repeated Start "1" : master repeated Start
1-0	-	-	

**Table 3 : Status Register (MBSR : \$93h)**

Bit Location	Name	$\mu$ C Access	Description
7	MCF	Read	Data Transferring Bit transfer : "1" transfer : "0"
6	MAAS	Read	Address as Slave Bit
5	MBB	Read	Bus Busy Bit bus busy : "1" bus idle : "0"
4	MAL	Read Software Clearable	Arbitration Lost Bit I <sup>2</sup> C bus is lost : "1" $\mu$ C write "0" : "0"
3	-	-	
2	SRW	Read	Slave Read/Write Bit "1" Master reading from Slave "0" Master writing to Slave
1	MIF	Read Software Clearable	Interrupt Bit
0	RXAK	Read	Received Acknowledge Bit "1" receive no ack "0" receive ack

**Table 4 : Data Register (MBDR : \$95h)**

Bit Location	Name	μC Access	Description
7-0	D7:D0	Read/Write	I <sup>2</sup> C Data

5. Timing Diagram

6. Clock Distribution

7. Bus interface & I/O configuration

**Table 5 : Top IO Signal Description**

Name	Direction	Description
SDA	I/O	I <sup>2</sup> C Serial Data
SCL	I/O	I <sup>2</sup> C Serial Clock
ADDR_BUS[23:0]	I	μC Address Bus
DATA_BUS[7:0]	I/O	μC Data Bus
AS_N	I	<b>Address Strobe</b> (active low) Address
DS_N	I	<b>Data Strobe</b> (active low) Data
R_W	I	<b>Read/Write</b> (active low) "1" Read reg. , "0" Write to reg.
DTACK_N	O	<b>Data transfer Acknowledge</b> (active low) receive cycle : μC data write cycle : μC data
IRQ_N	O	<b>Interrupt Request</b> (active low)
MCF	O	<b>Data Transferring Bit</b> 1byte data가 "0" "1"
CLK	I	<b>Clock</b>
RST_N	I	<b>Reset</b> (active low)

**Table 6 : uC Interface to EC Interface Signal Description**

<b>Name</b>	<b>Direction</b>	<b>Description</b>
RST_RSTA	I	<b>Repeat Start reset</b>
RST_MSTA	I	<b>MSTA bit reset</b> if Arbitration lost
MBSR[7:0]	O	<b>To I<sup>2</sup>C status register</b>
MBCR[7:0]	O	<b>Control register</b>
MADR[7:0]	O	<b>Address register</b>
MBDR_I2C[7:0]	I	<b>From I<sup>2</sup>C data register</b>
MBDR_MICRO[7:0]	O	<b>From uC data register</b>
RST_MAL_BIT	O	<b>MAL bit reset</b> if uC software writing "0"
RST_MIF_BIT	O	<b>MIF bit reset</b> if uC software writing "0"
MBCR_WR	O	<b>MBCR write enable</b> (maal bit reset if MBCR writing)

8. Test Description

9. Integration requirement

10. Version History

11. Known bug

12. Application note

13. Deliverable list / format