APPLICATION NOTE

Mentor Synthesis Group

Using Precision to design Rad-Hard Actel devices

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Abstract

A brief account is given of the recent work involving VLSI and programmable logic devices for heightened radiation environments. Actel antifuse programmable logic devices are found to be a suitable platform for these environments. Techniques are proposed to harden designs against radiation-induced soft errors. Finally, the radiation hardened mapping support in Mentor Graphics Precision™ RTL Synthesis is introduced.

Introduction

Antifuse programmable logic has been in use for fifteen years; throughout this time, Actel Corporation has been a leader in antifuse programmable logic devices. In 1988, Actel introduced the dielectric based antifuse for use in logic and memory ICs [1], as part of the first family of desktop-configurable channeled gate arrays.

As solar particle event models originally proposed in 1988 were revised in 1994 to better reflect observed densities of heavy ions during solar flares [4], these models allowed designers to consider a wider range of devices from standard commercial processes [5]. As time passed, and process geometries continued to shrink, it was observed that vulnerability to latch-up and single-event phenomena worsened, while total dose and displacement damage susceptibility tended to improve [2].

SRAM-based FPGAs have been the subject of numerous radiation susceptibility studies. In 1998, Xilinx 4000XL and 4000E family devices were subjected to nine hours of irradiation at a neutron energy of 100 MeV [6]. It was found that both device families exhibited relatively low susceptibility, with the 4000E family device encountering just one SEU and the 4000XL device encountering five. In 1999, engineers at Actel explored an SRAM-based architecture [7], also finding that total dose tolerance improves as feature size shrinks. However, Actel's findings suggested that the configuration SRAM exhibited unacceptably high susceptibility to SEUs, and hardening of these cells was found to be challenging.

Actel's antifuse programmable logic devices have been well characterized over time, and generally perform well in heightened radiation environments. A thorough characterization of Actel's ACT1 and ACT2 antifuse programmable logic device families [3], including Single Event Upset (SEU) susceptibility data for sequential (S) vs. combinatorial (C) modules, reported that the difference between the vulnerabilities of the C and S modules is substantial. C-module flip-flops were found to be about an order of magnitude less susceptible to SEUs than S-modules for a Linear Energy Transfer of up to ~ 60 MeV-cm^2/mg, with the difference lessening as LET increased beyond that point. Though SEUs were found to be of concern, clock line disruptions were found to be of lesser concern. No clock line disruptions were encountered during testing with an LET of ~ 25 MeV-cm^2/mg, and clock frequencies ranging from 2.5kHz to 10MHz.

This same report [3] found that a Triple Module Redundancy (TMR) circuit implementation on these devices was found to perform extremely well, correcting 44,538 monitored SEUs in the flip flops comprising the TMR cells. The authors made a recommendation that TMR structures be used for all critical control structures and datapath when designing with the S-modules. They also suggested that when operating in severe environments such as a solar flare, TMR circuits be used in conjunction with C-module flip-flops. The report finally claims that careful clock tree construction and logic placement will result in greatly reduced SEU vulnerability.

In addition to earlier recommendations for using TMR circuitry [3], numerous other studies have addressed radiation tolerant design techniques at the application level. In 2001, a simulation flow was proposed for upset-like fault injection in a VHDL hardware description [8], whereby every flip-flop in the design is replaced by an equivalent model having the same functional features but designed to allow fault injection at any clock cycle. The flow suggests that a similar synthesis flow might assist with fault tolerant design by easily allowing targeting macros, which implement a triple module redundant circuit. Most recently, designers have been exploring Hamming Code versus Triple Module Redundancy in programmable logic devices [9], finding that though the hamming code is more area efficient for memories and wider register

banks, TMR is more area efficient for control and datapath logic. In addition, TMR and hamming code were found to be equivalent in area efficiency for word widths up to 16 bits; TMR is always preferred for delay due to the smaller delay of voting circuits compared to the XOR gates in the hamming decode logic.

Precision™ RTL Synthesis Supports RadHard Design

Against this backdrop, Mentor Graphics is pleased to announce its newly released radiation hardened mapping support for Actel devices, allowing designers to use C-module pairs to implement flip-flops, or TMR circuitry using either S- or C-modules for even greater tolerance to increased radiation environments. Based on previous characterizations of their devices' heavy ion response ([3], [9] et. al.), Actel recommends three techniques for implementing the logic of sequential elements in radiation-hardened FPGAs: Combinatorial-Combinatorial (C-C), Triple Module Redundancy (TMR), and Triple Module Redundant C-C (TMR_CC).

Combinatorial-Combinatorial (C-C)

The C-C technique provides a way to avoid using the radiation-soft S-module flip-flop by combining two combinatorial cells with feedback.

Triple Module Redundancy (TMR)

TMR, or triple voting, is a register implementation technique whereby each register is implemented by three flip-flops (or latches) that "vote" to determine the true state of the register.

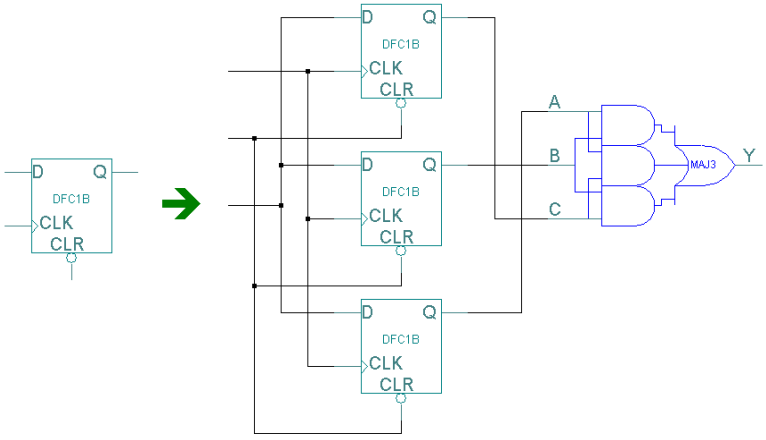

Figure 1 - Triple Module Redundancy register transformation

Triple Module Redundant C-C (TMR_CC)

TMR_CC is also a triple-module-redundancy technique where each voting register is composed of combinatorial cells with feedback instead of S-module flip-flop or latch primitives.

Steering Synthesis to use Radiation Hardened Implementations

In order to create a radiation hardened implementation, designers can set a "radhardmethod" attribute either on the reg/signal being driven by the flop, the flop instantiation itself, or on an entire module instantiation. Setting an attribute on the reg/signal being driven by the flop is made available to ease setting attributes in the HDL code. Each design object is able to inherit radhardmethod attributes from it's parent, providing a powerful yet intuitive approach to steering design implementation. In addition, a radiation-hardened implementation can be set for the entire design by issuing the command setup_design –radhardmethod=(one of "cc", "tmr", "tmr_cc", or "none").

Precision RTL Synthesis offers the highest possible level of control over radiation-hardened implementation, by allowing the designer to tailor attributes per design object instance. This method provides significantly better control than competing solutions, which only allow setting one implementation method for all instantiations of a design object by instrumenting synthesis metacomments in the HDL code. Not only does the Precision RTLSynthesis solution remove the dependency on instrumenting HDL code by

allowing attributes to be set in TCL scripts, the implementation offers far more flexibility in exploring trade-offs with highly folded designs.

Example TCL constraint:

```
# Setting attribute on a flop in a TCL file refers to the flop itself
set_attribute -name radhardmethod -value tmr_cc -instance
U1/reg_dataout

# Setting attribute on a module
set_attribute -name radhardmethod -value tmr -instance U2

# Setting rad hard method for the entire design
setup_design -radhardmethod=cc
```

Example Verilog Code:

```
// Setting the attribute on a reg through a Verilog synthesis directive

reg [7:0] dataout;

// pragma attribute dataout radhardmethod tmr_cc;

// Setting the attribute on an instantiated module
// through a Verilog synthesis directive

// pragma attribute U2 radhardmethod tmr;
```

Example VHDL Code:

```
-- Setting the attribute on a registered signal through a VHDL attribute
--
attribute radhardmethod : string;
attribute radhardmethod of dataout: signal is "tmr_cc";
--
-- Setting the attribute on an instantiated module
-- through a VHDL attribute
--
attribute radhardmethod : string;
attribute radhardmethod of U2: label is "tmr";
```

Saving the RadHardMethod in the Precision RTL Project

Once the setup_design command has been entered on the command line, a subsequent save of the project will automatically pick up the global implementation method setting. Attributes set on design objects will be saved to the designer's constraint file, for future reference and for synthesis.

Using the GUI to Set the RadHardMethod Attribute on an Object

Set the RadHardMethod Attribute by right-clicking on the design object in the Precision RTL Synthesis hierarchy browser, and selecting "Set Attributes…"

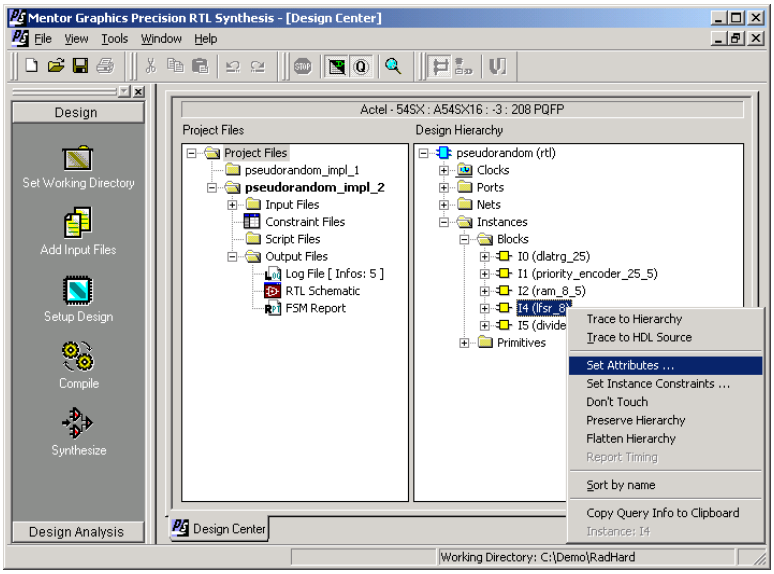

Figure 1 - Setting an attribute on a design object

Under User Attributes, select "New…"; enter "radhardmethod" as the attribute name, and set its value appropriately.

Figure 2 - Setting the "radhardmethod" attribute

Conclusion

Actel antifuse programmable logic devices are suitable for higher radiation environments; techniques exist for hardening designs against radiation-induced soft errors. Precision RTL Synthesis includes radiation hardened mapping support for Actel devices, allowing for even greater tolerance to increased radiation environments. For more information about radiation-hardened mapping support in Precision RTL Synthesis, contact your local sales representative, or visit http://www.mentor.com/synthesis

References

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