**Digital Design COEN 6501 Midterm exam. Oct 20th , 2014**

**Answer all questions. Time allowed 1 hr 30 min.**

**All questions carry equal mark A.J. Al-Khalili.**

**SAMPLE -- A**

**Question-1:**

Using array multipliers give a circuit for calculation of Y:

Y= **N**(2N)

where N is a 4-bit unsigned binary number.

Show this implementation for N=1011. Show the input to each adder clearly. Use “0” when an input is not connected.

**Question-2:**

Design an **4-bit Carry Look Ahead Adder**. Give delay performance of your adder. Show how you calculated your delay at gate level. Compare this to Carry Ripple Adder of the same size

***Assume*** all 2-input gates have tg delay. Further assume each extra fan –in adds 1/3 tg, and each added fan out adds ½ tg delay

**Question-3:**

1. Design a counter with the following repeated binary sequence 1 3 5 7. Start with a state diagram and follow design procedure in each step ending with the designed counter diagram.