**Question 1**

a)

FPGA’s have several advantages some are:

1. Ease of prototyping
2. Fast prototyping
3. Low cost of prototyping
4. Re-programmability
5. Availability of variety of FPGAs with embedded units
6. Availability and friendliness of tools
7. Fast testing of the circuit

b)

F(A,B,C,D,E,F,G,H) = $ABC+\overbar{A}BE+BCFGH+CDFH+A\overbar{C}FG$

F can be implemented with a variety of 2,3 and 4 variable LUT. In here, we give 2 implementations selected due to their lowest delay.

$$\overbar{A}$$

$$\overbar{D}$$

|  |  |  |
| --- | --- | --- |
| Delay |  | Area |
| 4 |  | $$4\*3LUT$$ |
| 2 |  | $$4\*2LUT$$ |
| 3 |  | $$2\*4LUT$$ |
| 9$ns$ |  | 124$mm^{2}$ |





$$\overbar{F}$$

$$\overbar{C}$$

$$\overbar{A}$$

$$\overbar{D}$$

|  |  |  |
| --- | --- | --- |
| Delay |  | Area |
| 2 |  | $$4\*3LUT$$ |
| 2 |  | $$4\*2LUT$$ |
| 2 |  | $$1\*4LUT$$ |
| 3 |  |  |
| 9$ns$ |  | 98$mm^{2}$ |

The second implementation has the same delay, but the better area.

**Question 2**

$$x.y-z=\left(x.y\right)+(-z)$$

$Z=Z\_{3} Z\_{2} Z\_{1} Z\_{0}$ Z is inverted and it is added to one get its –ve value and NOT XORed since we want is –ve.

$$Z=\overbar{Z\_{3} Z\_{2 }Z\_{1 }Z\_{0}}$$

 1+

 extension …. $\overbar{Z\_{3}Z\_{3}Z\_{3}}$

$$Z\_{3}$$

$Z\_{3} Z\_{2} Z\_{1}$ $Z\_{0}$



 +1

$$\overbar{Z\_{3}}\overbar{Z\_{3}}\overbar{Z\_{3}}\overbar{Z\_{3}}$$

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  | $$X\_{3}$$ | $$X\_{2}$$ | $$X\_{1}$$ | $$X\_{0}$$ |  |
|  |  |  |  |  | $$Y\_{3}$$ | $$Y\_{2}$$ | $$Y\_{1}$$ | $$Y\_{0}$$ |  |
|  |  |  |  |  | $$P\_{03}$$ | $$P\_{02}$$ | $$P\_{01}$$ | $$P\_{00}$$ |  |
|  |  |  |  | $$P\_{13}$$ | $$P\_{12}$$ | $$P\_{11}$$ | $$P\_{10}$$ |  |  |
|  |  |  | $$P\_{23}$$ | $$P\_{22}$$ | $$P\_{21}$$ | $$P\_{20}$$ |  |  |  |
|  |  | $$P\_{33}$$ | $$P\_{32}$$ | $$P\_{31}$$ | $$P\_{30}$$ |  |  |  |  |
|  | $$Z\_{3}$$ | $$Z\_{3}$$ | $$\overbar{Z}\_{3}$$ | $$\overbar{Z}\_{3}$$ | $$\overbar{Z}\_{3}$$ | $$\overbar{Z}\_{2}$$ | $$\overbar{Z}\_{1}$$ | $$\overbar{Z}\_{0}$$ |  |
|  |  |  |  |  |  |  |  | 1 | $$\leftarrow +1$$ |

$$M\_{8}$$

Critical Path

H

H

H

+

H

H

+

+

+

+

+

+

+

+

+

+

+

+

+

+

+

H

$$\overbar{Z}\_{3}$$

$$Z\_{3}$$

$$\overbar{Z}\_{3}$$

$$\overbar{Z}\_{2}$$

$$M\_{7}$$

$$M\_{6}$$

$$M\_{5}$$

$$M\_{4}$$

$$M\_{3}$$

$$M\_{2}$$

$$M\_{1}$$

$$M\_{0}$$

$$\overbar{Z}\_{3}$$

$$P\_{33}$$

$$\overbar{Z}\_{1}$$

$$P\_{00}$$

$$\overbar{Z}\_{0}$$

1

$$Critical Path=8τ\_{F}+τ\_{AND}$$

**Question 3**

|  |  |  |  |
| --- | --- | --- | --- |
| Present State | Next State |  |  |
| $$y\_{3}$$ | $$y\_{2}$$ | $$y\_{1}$$ | $$y\_{0}$$ | $$y\_{3}^{+}$$ | $$y\_{2}^{+}$$ | $$y\_{1}^{+}$$ | $$y\_{0}^{+}$$ |  |  |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |  | $$P\_{1}^{+}$$ |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |  | $$P\_{2}^{+}$$ |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |  | $$P\_{3}^{+}$$ |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |  | $$P\_{4}^{+}$$ |



From the table above:



|  |  |  |
| --- | --- | --- |
| $$P\_{1}^{+}=P\_{2}$$ |  | $$y\_{3}^{+}=y\_{0}$$ |
| $$P\_{2}^{+}=P\_{3}$$ |  | $$y\_{2}^{+}=y\_{3}$$ |
| $$P\_{3}^{+}=P\_{4}$$ |  | $$y\_{1}^{+}=y\_{2}$$ |
| $$P\_{4}^{+}=P\_{1}$$ |  | $$y\_{0}^{+}=y\_{1}$$ |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| $y\_{3}y\_{2}$ $y\_{1}y\_{0}$ | 00 | 01 | 11 | 10 |
|  00 |  | 1 | X |  |
| 01 |  | X | X |  |
| 11 |  | X | X |  |
| 10 |  | X | X |  |

$$y\_{3}^{+}=y\_{0}$$

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| $y\_{3}y\_{2}$ $y\_{1}y\_{0}$ | 00 | 01 | 11 | 10 |
|  00 |  |  |  |  |
| 01 |  |  |  |  |
| 11 | X | X | X | X |
| 10 | 1 | X | X | X |

$$y\_{2}^{+}=y\_{3}$$

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| $y\_{3}y\_{2}$ $y\_{1}y\_{0}$ | 00 | 01 | 11 | 10 |
|  00 |  |  |  |  |
| 01 | 1 | X | X | X |
| 11 | X | X | X | X |
| 10 |  |  |  |  |

$$y\_{1}^{+}=y\_{2}$$

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| $y\_{3}y\_{2}$ $y\_{1}y\_{0}$ | 00 | 01 | 11 | 10 |
|  00 |  |  | X | 1 |
| 01 |  |  | X | X |
| 11 |  |  | X | X |
| 10 |  |  | X | X |

$$y\_{0}^{+}=y\_{1}$$

**Question 4**

a)



There are 6 paths:

Path1: $u\_{1}-u\_{2}-u\_{4}-u\_{6}$

Path2: $u\_{6}-u\_{7}-u\_{8}$

Path3: $u\_{8}-u\_{10}-u\_{12}$

Path4: $u\_{1}-u\_{2}-u\_{5}-u\_{7}-u\_{8}$

Path5: $u\_{8}-u\_{11}-u\_{2}-u\_{4}-u\_{6}$

Path6: $u\_{8}-u\_{11}-u\_{2}-u\_{5}-u\_{7}-u\_{8}\leftarrow By inspection and calculation Critical path$

$$u\_{5}$$

$$u\_{2}$$

$$u\_{11}$$

$$u\_{8}$$

$CL\_{6}=0.2\left(1.5+1.5\right)+2+0.25\*1.5+2.5+0.25\*\left(1.5+1.5\right)+2.0+0.25\*1.5+2.5+0.25\*1=11.35ns$

$$u\_{7}$$

$$T\_{max}=3+11.35+1.5=15.85ns$$

$$S\_{o}f\_{max}=\frac{1}{T\_{max}}=\frac{1}{15.85}=63.1MHz$$

b)

Path delay at point D, $u\_{6}$ which is path 5.

$0.2\left(1.5+1.5\right)+2+0.25\*1.5+2.5+0.25\*\left(1.5+1.5\right)+2\*0.25\*1=8.47ns+3=11.47=T^{'}$

$$T\_{setup slack}=\left(T\_{max}-T\_{su}\right)-T^{'}=15.85-1.5-11.47=0.875ns$$

$T\_{hold}$ at point D, $u\_{6}$ is

$$T\_{h\_{max}}<T\_{CQ\_{min}}+T\_{CL\_{min}}-T\_{CS\_{max}}$$

$T\_{CL\_{min}}$ is path 1 delay, $T\_{CQ\_{min}}=3$, $T\_{CS\_{max}}=0$,$ CL\_{path1}=8.65$

$$∴ T\_{h}=3+8.65-0=14.47$$

$$T\_{h slack}=11.65-0.5=11.15ns$$

c)

When clock skew is introduced between $u\_{1}$ and the rest. We calculate the changes to the path. Path 4 is the longest path.

$$T\_{path4}=0.2\left(1.5\right)+2+0.25\left(1.5+1.5\right)+2+0.25\*1.5+2.5+0.25\*1+T\_{int\_{ff}}+T\_{su}=13.175+3.5=16.67ns$$

New critical path has been introduced. This is the added delay at the input of $u\_{2}$ since CLK of other FFs is taken as a reference.

$$T\_{path4}>T\_{path6}$$

$$New frequency=\frac{1}{16.67}=59.001 MHz$$

**Question 5**

a)

Typical Delays

$t\_{NAND}=0.25+0.03\*1.5=0.295 ns$

@ Ambient temp of 27$℃$

$$t\_{XNOR}=0.4+0.05\*2=0.5 ns$$

$$t\_{MUX}=0.3+0.1\*2=0.5 ns$$

$$t\_{FF}=0.5+0.07\*1.5=0.605 ns$$

Delay Variations

$k\_{v}=\frac{1}{1+0.01f\_{0}}=\frac{1}{1\pm 0.01×10}=1.11$ , 0.909 voltage variation

$k\_{T}=t\_{a}+θ\_{Ja}\*P\_{J}$

$\left(T\_{2}\right)\_{min}=-55+30\*3=35℃+273=308°K$

Junction Temp Variation

$$\left(T\_{2}\right)\_{max}=125+30\*3=215℃+273=488°K$$

$\left(k\_{T}\right)\_{min}=\left(\frac{308}{27+273}\right)^{1.5}=+1.05$

De-rating Temp Variation

$$\left(k\_{T}\right)\_{max}=\left(\frac{488}{27+273}\right)^{1.5}=+2.09$$

Composite De-rating factor $K^{'}=K\_{v}\*K\_{T}$

$$K^{'}\_{min}=0.909\*1.05=0.954$$

$$K^{'}\_{max}=1.11\*2.09$$

Min/Max delay

$$t\_{NAND}=0.281ns, 0.684 ns$$

$t\_{XNOR}=0.477ns, 1.16 ns$

Min, Max Delay of the Gates used in Figure 2

$$t\_{MUX}=0.477ns, 1.16 ns$$

$$t\_{FF}=0.58ns, 1.4 ns$$



D-input



Latest arrival

$$\leftarrow $$

3.004

1.057



$$t\_{s}$$

b)

Total Period $T=T\_{CQ\_{max}}+T\_{CL\_{max}}+T\_{su\_{max}}-T\_{CS\_{min}}$

$$T\_{max}=1.4+3.004+0.2-0=4.604ns$$

$$f=\frac{1}{T}=\frac{1}{4.604}=217 MHz$$

**Question 6**

a)

There are many ways of writing this piece of code. Here is just a simple example:

library IEEE;

use IEEE.std\_logic\_1164.all;

entity exam\_circuit is

port (A, B : in std\_logic;

 O1,O2 : out std\_logic);

end exam\_circuit

architecture structural of exam\_circuit is

component decoder2to4

port(a, b : in std\_logic;

 d1, d2, d3, d4 : out std\_logic);

end component decoder2to4;

component AND\_gate

port(in1, in2 : in std\_logic;

 out1 : out std\_logic);

end component AND\_gate;

component OR\_gate

port(in1, in2 : in std\_logic;

 out1 : out std\_logic);

end component OR\_gate;

signal d1, d2, d3, d4 : std\_logic;

begin

decoder1: decoder2to4 portmap (A, B, d1, d2, d3, d4);

AND1 : AND\_gate portmap (d1, d2, O1);

OR1 : OR\_gate portmap (d3,d4, O2);

End structural

b)

L2: X,Y : I std\_logic

L4: end Half\_A\_Con

L5: H\_A\_Behav

L7: -signal

L8: process(X,Y)

L13: problem of conversion X,Y

L17: endif