ECE 4170: Introduction to Hardware Description Languages with Applications to Digital Design

Course Content: Goals

• Understand the concepts underlying hardware description languages
  – Roles and application in digital design flows
  – Key language features: what is represented and why

• Reinforce language concepts with a significant project component
  – Place the project in the context of modern system-on-chip design

• Use VHDL as the working language
  – Introduction to competing, alternative languages
  – Understand commonality with VHDL as well as rationale for their distinct language features
Course Content: Goals (cont.)

- Learn and apply industry standards
  - Open core protocol (OCP)
    - Standard for Intellectual property (IP) integration
    - SPIRIT: standard for describing IP metadata
  - 1076.6 IEEE Standard for VHDL RTL Synthesis

- System-on-Chip project infrastructure
  - Leverage available SoC infrastructures
    - OpenRISC
    - MicroBlaze

System Architecture

Program Memory

mpeg_program.rom

OpenRISC CPU

Register File

CPU fetches program instructions

Data Memory

Input Data for processing

Data from supplied program

Results produced

Data from

mpeg_data.init

Custom Hardware

- MPEG decoder

Program and data memories initialized from files at start of simulation.
Data memory dumped to file at end.

Wishbone Bus

Base address Slave-1: 0x0000_0000
Base address Slave-2: 0x0100_0000

Program and data memories initialized from files at start of simulation.
Data memory dumped to file at end.

CPU reads, writes data

mpeg_data.init

sram0.dump

CPU reads, writes data

gpr.log
Verilog + VHDL

- Program Memory
- OpenRISC CPU
- Data Memory
- Wishbone Bus
- Custom Hardware
  - MPEG decoder
  - Vector machine
  - Encrypted I/O

In **VHDL**: Create entity for Custom Hardware 
(different for each custom-hardware)

In **Verilog**: Do component-instantiation and port-map

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Industry’s Challenges

- Escalating costs and time to market of silicon platforms
  - Mask costs
  - Manufacturing
  - Verification
  - Design
- Escalating design complexity
  - Number of transistors
  - Deep submicron effects
  - Application complexity in emerging markets
- Need for hardware customization
  - To concurrently meet physical, functional, and cost requirements
Industry Response

• Raise the level of design abstraction
  – Emergence of Electronic System Level (ESL) Design
    • Algorithm-based RTL synthesis

• Raise the level of hardware building blocks
  – Processors, memories, cores, etc.
  – Configurable fabrics
  – Emergence of System-on-Chip (SoC) platforms

• IP–Reuse
  – In design: For example ARC, ARM and Artisan
  – In manufacturing: For example NEC and eASIC

Semiconductor Market Drivers: 2006-2009

• Integration:
  – A byproduct of Moore’s Law

• Manufacturing
  – Emergence of design for manufacturing

• Consolidation
  – Emergence of new design processes

• Costs
  Design and IP will become the primary differentiators
Opportunity

- Emergence of derivative SoC Platforms
  - 10s of platforms but thousands of derivative platforms
  - Derivatives couple application specific logic with commodity component-based platforms

- Growth in consumer markets
  - OEMs need complete solutions to focus on product differentiation in short product development cycles

- Exploding pool of accessible embedded software developers
  - Access to geographically distributed SoC IP generation capability

- Fragmented derivative SoC development flow
  - Weak link between ESL and RTL for design
  - Fragmented software development tool chain and environment

Major Market Drivers

- Consumer
  - Home entertainment, cell phones, intelligent imaging, gaming

- Communications
  - Wireless, VoIP, video conferencing, cell phones

- Emphasis on power/performance balance

- New (commodity) design processes that
  - Make use of distributed intellectual capital → lower the expertise barrier
  - Collaboration (horizontal) is more important than top-down control (vertically directed) of design
  - Open source & standards (C, Spirit, OCP, etc) is the vehicle
  - Design/IP is the driver/differentiator rather than manufacturing
**Landscape**

**Design NRE Effort**

- Decreasing Customization
- Increasing NRE and Time to Market

- **Hardware-Based**
  - Custom ASIC
  - Structured ASIC
  - FPGA
  - Configurable Fabrics
  - Tiled architectures

- **Algorithm-Based Design Flow**

- **Software-Based**
  - Fixed + Variable ISA
  - Microprocessor

**Market Sizes**

- **ASICs will outgrow semiconductor industry 2006 (Gartner)**
  - One-third will be structured ASICs by 2008
  - $2B market by 2007
  - Altera and LSI Logic are market leaders
  - ~$200M - $300M tools market

- **Electronic System Level (ESL) design tools will be $1.6B by 2009 (Gartner)**
  - Companies reliance in internal ESL tools increased 33% in 2005

- **Capture 10%-20% of the FPGA market**
  - ~$5B in 2007
The Challenge: SoC Design

- Modern System-on-Chip Design is dominated by intellectual property (IP) re-use
- Chip complexity is spread across multiple design groups in multiple companies, and even across multiple market segments
- Large fraction of time is spent on integration and testing → emergence of industry standards for IP integration

Example

From M. Jacome, UT Austin
**Course Logistics**

- **Instructor:** Professor Sudhakar Yalamanchili
  - Class webpage for contact information: [www.ece.gatech.edu/users/sudha/4170/Spring2007](http://www.ece.gatech.edu/users/sudha/4170/Spring2007)
  - Recommended Text: *VHDL: From Simulation to Synthesis*, S. Yalamanchili, Prentice Hall (pubs.)
  - The following will be provided:
    - Class notes
    - Alternatives to the recommended text
    - Supplemental reading

- **Teaching Assistant:** TBA

- **Infrastructure**
  - ECE Linux Clusters in the College of computing building
    - Simulation: Modelsim
    - Synthesis: Mentor Graphics Leonardo Spectrum or Synplicity
  - Tutorials will be provided

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**AMD Au1200 System on Chip**

- Embedded processor
- Custom cores
- On-Chip I/O
- On-Chip Buses

Source: AMD
Evaluation

- Midterms: 2, 20% each
  - 24 hour take home examination
- Assignments: 20%
- Final/Project: 40%
  - Group projects will be considered
  - Detailed description of milestones will be provided
    - Schedule, format, and content
  - Presentation during final examination
  - Final oral examination