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Project Name: rs232

Creation Date: May 2003

Development Board: XESS XSA-100 Plus XStend Version 2

Development Software: Xilinx ISE Version 5.1.03i

Description

This project demonstrates how to interface the rs232 port to a terminal/computer. To use, connect a null modem cable from a PC com port to XStend's rs232 port. The only requirement of the null modem cable is that receive and transmit signals are crossed, and ground is wired. All flow control signals such as cts and rts are ignored.

Use a simple terminal emulator such as HyperTerminal (provided with Windows) and set terminal to the appropriate com port with settings of 9600 baud, 8 data bits, no parity, 1 stop bit and no flow control.

The top-level vhdl entity is chipIO. It serves as the primary interface between the design and the external IO pins on the fpga. Many more pins than are required for this project are declared in this interface and the accompanying ucf file. Those pins are ignored.

The heart of the design consists of declaring an instance of the uart and a single process statement to effectively echo keyboard characters received through the interface back out the rs232 connection to the pc com port. Characters are buffered when received, then transmitted as soon as the transmitters buffer is available.

The design is set to run at 10MHz. Make sure the external oscillator is programmed for this frequency. This is the only requirement due to the fact that the baud rate generator needs to run at the correct frequency. A generic is provided to change this if a different external freq is provided.

This project utilizes the VHDL based MiniUART core available at www.opencores.org. Documentation for the uart core itself is provided as originally obtained from the opencores site.

Project Directory Structure

This project is organized into the following directories:

./ - contains all the files need to synthesize the design.

./config – effectively a backup of all main files in the root directory

./docs – this PDF file. Source files used to build this PDF are located in ./docs/src.

./ref – reference directory. Contains original hdl code used in design as downloaded from source.

./src – source directory for all HDL files

./temp – temporary directory used during the build process.

Synthesis

The project is built and maintained using two windows based batch files. The first is “make.bat”. It simply issues are the commands required to “compile” all the source files in the ./src directory and eventually generate the chipIO.bit file to downloaded to the fpga.

The second batch file is called “clean.bat”. Its sole purpose is to delete most of the unwanted files generated during the build process.