XAPP709 (v1.1) November 16, 2004

DDR SDRAM Controller Using Virtex-4 FPGA Devices

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Summary

This application note describes a 200-MHz DDR SDRAM (JEDEC DDR400, PC3200 standard) controller implemented in a Virtex-4™ XC4VLX25 FF668 -10CES device. This implementation uses direct clocking for data capture and an automatic calibration circuit to adjust delay on the data lines.

DDR SDRAM devices are low-cost, high-density storage resources that are widely available from many memory vendors. This reference design has been developed using DDR400 SDRAM components and DIMMs.

DDR SDRAM Description

The DDR SDRAM specification details are available from JEDEC organization, part of the Electronic Industries Alliance (EIA), at http://www.jedec.org/. The DDR SDRAM specifications are published in the JEDEC document, under the reference JESD79C.

DDR SDRAM devices are the silicon memory resource most frequently used in systems today, with applications ranging from consumer products to video systems. DDR SDRAM device frequencies range to 200 MHz, or DDR400. DRAM devices are available in component or module configurations.

DDR Controller Commands

Table 1 presents the commands issued by the controller. These commands are passed to the memory using the following control signals:

- Row Address Select ($\overline{RAS}$)
- Column Address Select ($\overline{CAS}$)
- Write Enable ($\overline{WE}$)
- Clock Enable (CKE) (always held High after device configuration)
- Chip Select ($\overline{CS}$) (always held Low during device operation)

Table 1: **DDR SDRAM Commands**

Signal No.	Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
1	Load Mode Register	L	L	L
2	Auto Refresh	L	L	H
3	Precharge(1)	L	H	L
4	Select Bank Activate Row	L	H	H
5	Write Command	H	L	L
6	Read Command	H	L	H

Table 1: **DDR SDRAM Commands *(Continued)***

Signal No.	Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
7	No Operation (NOP)	H	H	H

Notes:

1. Address signal A10 is held High during PRECHARGE ALL BANKS and is held Low during single bank precharge.

Command Functions

Mode Register

The mode register is used to define the specific mode of DDR SDRAM operation, including the selection of burst length, burst type, CAS latency, and operating mode. Figure 1 shows the Mode Register features that this controller uses.

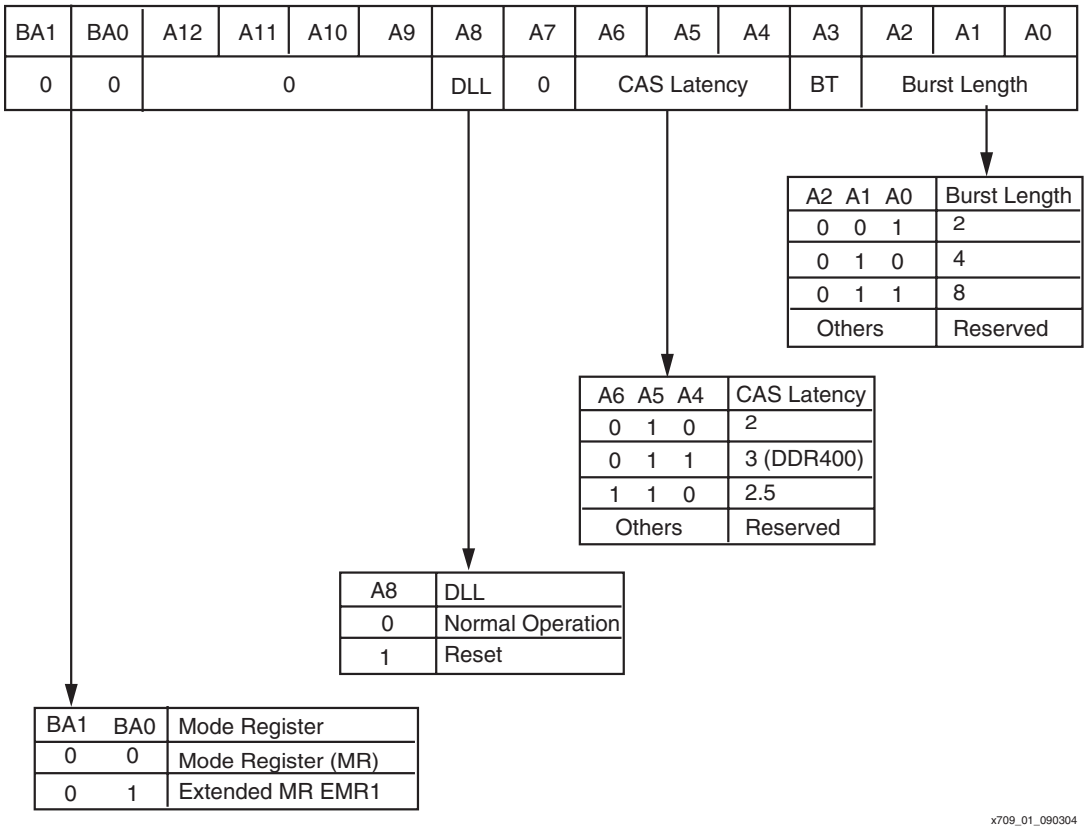

Figure 1: **Mode Register Definition for DDR400**

Bank Addresses BA1 and BA0 select the mode registers. Figure 1 shows the Bank Address bits configuration.

Extended Mode Register

The Extended Mode Register controls functions beyond those controlled by the Mode Register. These additional functions are DLL enable/disable and output drive strength for DDR SDRAM interfaces shown in Figure 2.

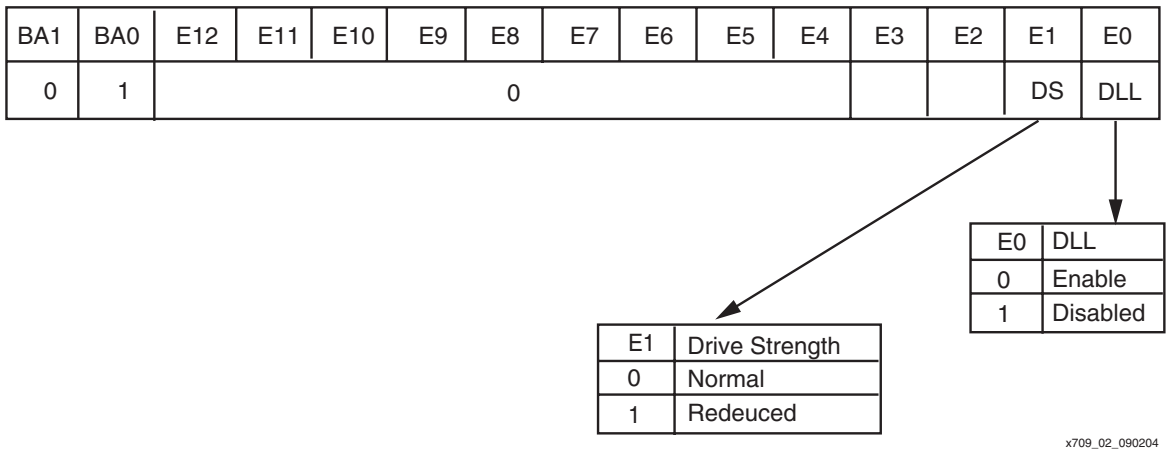

Figure 2: **Extended Mode Register for DDR400**

Initialization Sequence

The Initialization Sequence used in the controller state machine follows the DDR SDRAM specifications. The configuration sequence is split in two steps: the first step is handled by the hardware at power-up; the second step is handled by the FPGA memory controller design. Figure 3 shows the sequence of commands issued for initialization.

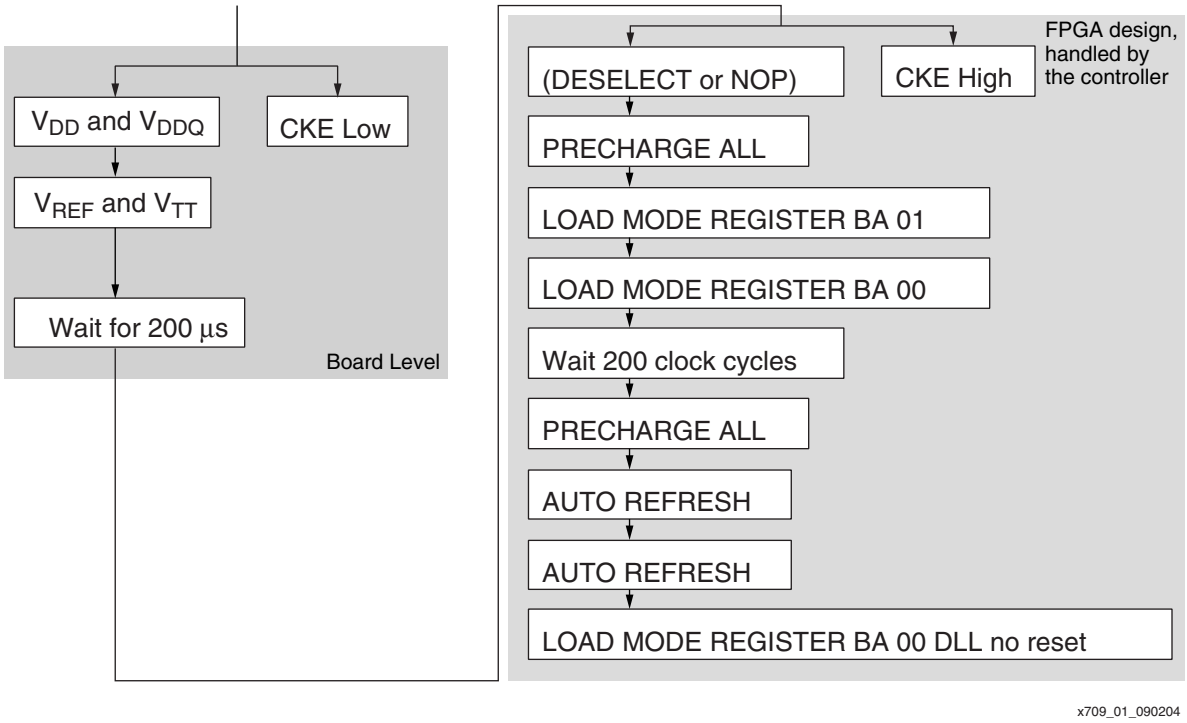

Figure 3: **Initialization Sequence for DDR SDRAM with Virtex-4 Device**

After the above sequence is complete, the controller issues dummy Read commands to the DDR SDRAM memory device. This process allows the data path module to select the right number of taps in the Virtex-4 input delay block. The data path module uses the Data Strobe (DQS) issued by the memory during this dummy Read command period to determine the relationship between the incoming Data Strobe (DQS) to the internal system clock (CLK0). After the data path module has determined the right number of delay taps required, a Tap_select_done signal is issued to the controller. The controller then goes into IDLE state.

PRECHARGE Command

The PRECHARGE command is used to deactivate the open row in a particular bank. The bank is available for subsequent row activation for a specified time (t_{RP}) after the precharge command is issued. Input A10 determines whether one or all banks are precharged.

Auto Refresh Command

DDR SDRAM devices must be refreshed every 7.8 µs maximum. Otherwise, data stored in the memory device can be lost. The controller contains the Auto Refresh command circuitry. This module uses a system clock divided by 16 outputs for the refresh counter. Auto_ref is the signal that flags the need for Auto Refresh commands when it is asserted. The auto_ref signal is held High 7.8 µs after the previous Auto Refresh command. The controller then issues the Auto Refresh command after it has completed its current burst. Auto Refresh commands always have highest priority in this design version.

ACTIVE Command

The ACTIVE command activates a row in a bank, allowing any READ or WRITE commands to be issued to a bank in the memory array. After a row has been opened, READ or WRITE commands can be issued to that row, subject to the t_{RCD} specification. When the controller detects an incoming address that refers to a row in a bank other than the currently opened row, the controller issues an address conflict signal. The controller then issues a PRECHARGE command to deactivate the open row and then issues another ACTIVE command to the new row.

Read Command

The Read command is used to initiate a burst read access to an active row. The value on BA0 and BA1 selects the bank address. The address inputs provided on A0 – Ai select the starting column location. After the read burst is over, the row is still available for subsequent access until it is precharged.

Figure 4 shows the case of a READ command with an additive latency of zero. Hence, the Read latency in this case is the same as the CAS latency which is 3 in the DDR400 specification.

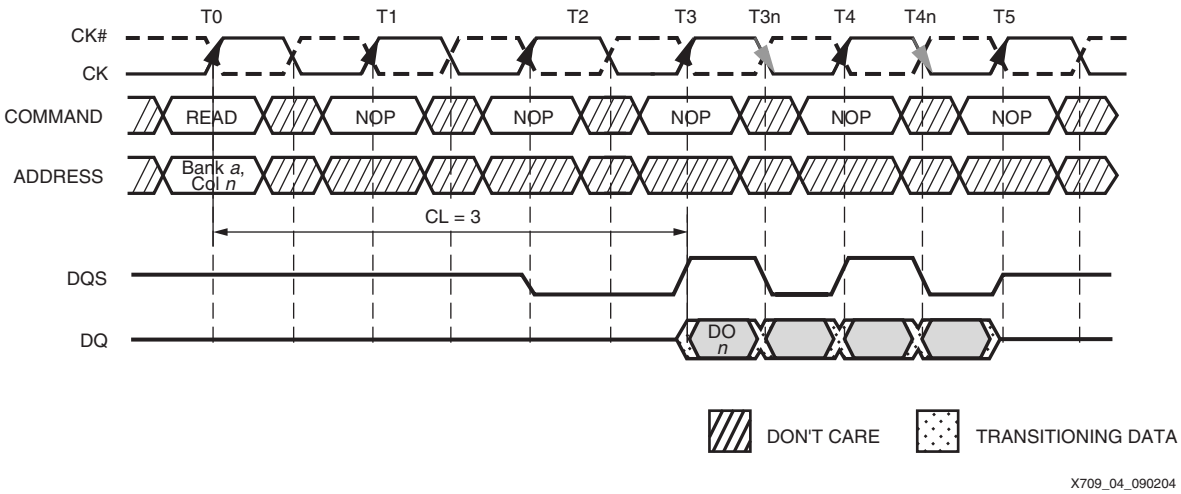

Figure 4: **DDR SDRAM Read Access Waveforms**

Write Command

The WRITE command is used to initiate a burst access to an active row. The value on BA0 and BA1 selects the bank address, while the value on address inputs A0 – Ai selects the starting column location in the active row. The value of Write Latency for DDR SDRAM devices is equal to Read Latency minus one clock cycle.

```
Write Latency = Read Latency -1 = CAS Latency -1.
```

Figure 5 shows a Write burst with a Write Latency of two. The time between the WRITE command and the first rising edge of the DQS signal is determined by the Write Latency.

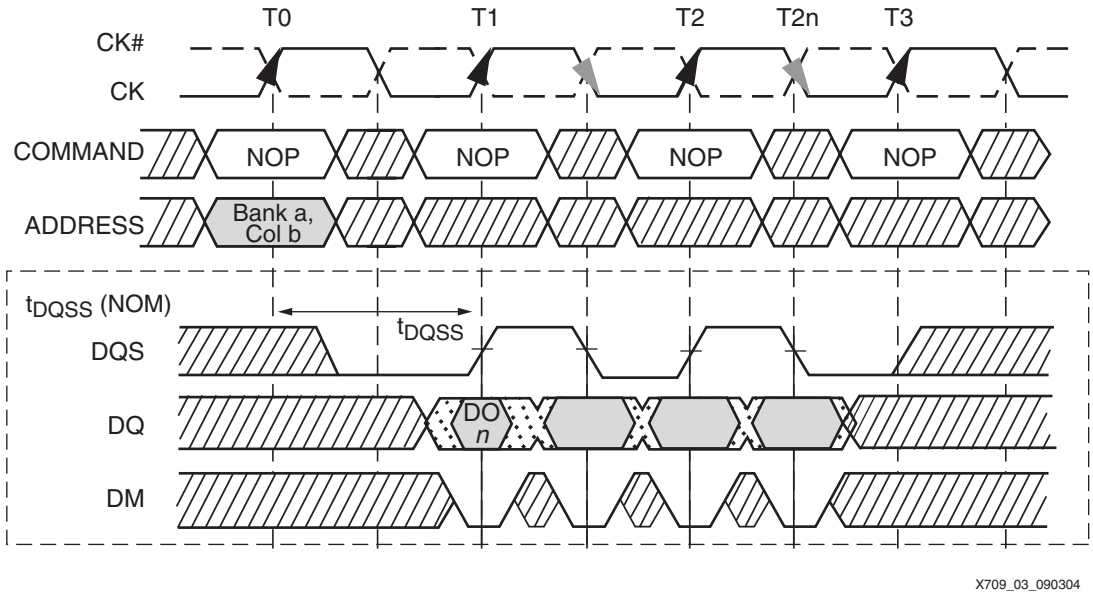

Figure 5: **DDR SDRAM Write Command Waveform**

DDR SDRAM Interface Implementation

This section presents the characteristics of the DDR SDRAM controller and interface, the interface block diagram (Figure 6), and the controller state machine (Figure 7).

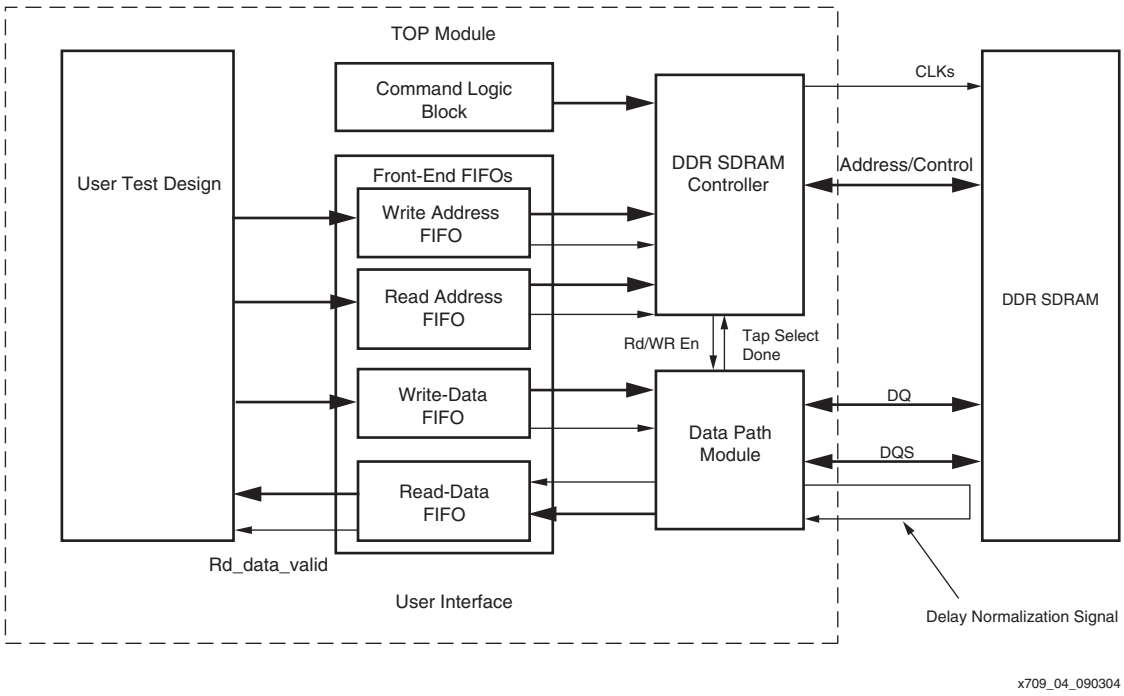

Figure 6: **Controller Design Block Diagram**

Hardware Testbench

The hardware testbench provides address and data patterns to test all the design aspects of the DDR SDRAM controller. The user backend includes the following blocks: backend state machine, read data comparator, and a data generator module. The data generation module generates the various address and data patterns that are written to the memory device. The address locations are pre-stored in a block RAM and used here as a Read Only Memory (ROM). The address values stored have been selected to test accesses to different rows and banks in the DDR SDRAM device. The data pattern generator includes a state machine issuing data patterns. The backend state machine serves in the role of user test design and issues the Write or Read Enable signals to determine which FIFO needs to be accessed by the data generator module.

User Interface

The backend user interface is comprised of four FIFOs, namely the Write Address FIFO, the Write Data FIFO, the Read Address FIFO, and the Read Data FIFO. The first three FIFOs are accessed by the user backend modules, while the Read Data FIFO is accessed by the data path module to store the captured Read data.

Command Logic Block

The command logic block provides commands to the controller. The user can modify it with their own command-generation module or replace it with a command FIFO. The command-generation module used in this design generates alternate Read and Write commands. The command logic block is a simple state machine which issues the commands to the controller.

DDR SDRAM Controller Interface

Figure 7 presents the state machine of the DDR SDRAM command generation state machine.

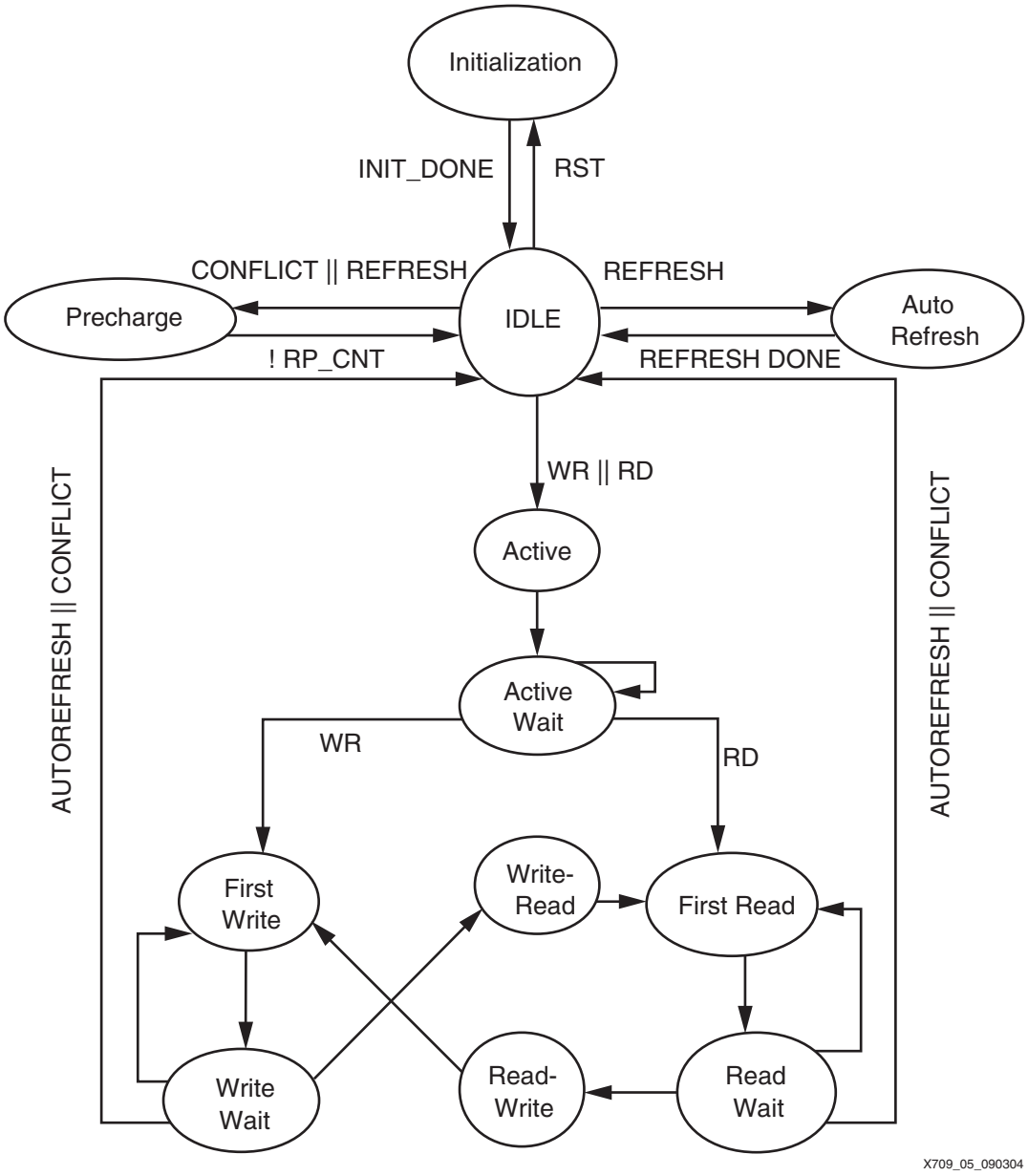

Figure 7: **DDR SDRAM Controller State Machine**

These are the steps that are followed before the controller issues the commands to the memory:

1. The command logic block generates a Write/Read command.
2. The controller issues a Read Enable signal to the Write/Read Address FIFO.
3. The controller activates a row in the corresponding bank if all banks have been precharged or compares the bank and row addresses to the already open row and bank address. If there is a conflict, the controller precharges the open bank and then issues an ACTIVE command before moving to the READ/WRITE states.
4. Once in the WRITE state, if the controller sees a READ command, the controller waits for the write_to_read time before issuing the READ command. Similarly, in the READ state,

when the controller sees a WRITE command from the command logic block, the controller waits for the read_to_write time before issuing the WRITE command.

5. The commands are pipelined to synchronize with the Address signals before being issued to the DDR2 memory.

Reference Design Specifications

The reference design package is available on the Xilinx web site at:

http://www.xilinx.com/bvdocs/appnotes/xapp709.zip

The design has been hardware verified at frequencies higher than 200 MHz. Table 2 provides the reference design specifications,

Table 2: **Reference Design Specifications**

Parameter	Specifications/Details
Frequency of operation	200 MHz (DDR400 – PC3200)
Virtex-4 device speed grade	10
Device utilization for full design interface	TBD
Number of slices for DIMM interface only	TBD
Number of slices for component interface only	TBD
Supported burst modes	4, 8
HDL language	Verilog, VHDL
Bus width	Component 16 bits, DIMM 144 bits
Device used for verification for components	Micron MT46V32M16
Device used for verification for DIMMs	Micron MT18VDDF6472AG-40BG4

Design Files

Table 3 lists the reference design files:

Table 3: **Design File List With Descriptions**

Module Name	Description of Each Module
top.v	Top level module for the DDR controller and Physical Layer
clk_module.v	Instantiates the DCM_BASE primitive for the memory interface, and the 200 MHz clock for the IDELAYCTRL module
data_path.v	Top level for the physical layer. Instantiates the following modules: tap_ctrl, data_tap_inc, idelay_ctrl, idelay_rd_en, v4_dqs_iob, v4_dq_iob, and rd_data_fifo.
data_tap_inc.v	Implements the tap selection controller for data bits associated with a strobe.
idelay_ctrl.v	Instantiates the IDELAYCTRL primitive required when the IDELAY primitive is used in the design.
idelay_rd_en.v	Instantiates the IDELAY primitive and IOB flip-flops for the normalized read enable signal.

Table 3: **Design File List With Descriptions *(Continued)***

Module Name	Description of Each Module
tap_ctrl.v	This module detects two transitions of a dqs (strobe) signal and determines the tap delay required for the associated data bits in order to center them with respect to internal FPGA clock, CLK
v4_dm_iob.v	Instantiates the IDELAY primitive and IOB flip-flops for the bi-directional data.
v4_dq_iob.v	Instantiates the IDELAY primitive and IOB flip-flops for the bi-directional data.
v4_dqs_iob.v	Instantiates the IDELAY primitive and IOB flip-flops for the bi-directional strobe.
controller.v	• Provides the read enable signals to the Write Address, Write Data and the Read Address FIFOs • Includes the controller state machine. Supplies the right command signals to the DDR2 device. Auto Refresh commands are generated by the controller taking the Auto Refresh Command Interval into account. • Provides the address signals to the DDR2 device.
test_bench.v	Synthesizable test bench for the memory interface.
backend_rom.v	Stores the data and address to be written and accessed in the memory array.
cmp_rd_data.v	Generates the error signal in case of bit errors. It compares the read data with expected data value.
user_interface.v	Instantiates the FIFO16 primitive for read data. One FIFO for rising-edge data and the other for falling-edge data.
backend_fifo.v	Instantiates the backend FIFOs for the DDR SDRAM interface. This includes the write address and data FIFOs, and the read address and data FIFOs. The FIFOs are implemented using the Virtex-4 FIFO16 primitives or FIFO made from LUT RAM instances.
Command_logic.v	Constitutes an arbiter for the interface. The user can modify in the module the conditions for read and write accesses for example.
Rd_data_fifo.v	Instantiates the FIFO16 primitive for read data. One FIFO for rising-edge data and the other for falling-edge data.

Design Hierarchy

The following tree summarizes the hierarchy in the reference design:

```
top_tb
   top
      controller
   clk_module
   data_path
   user_interface
      backend_fifos_36
      backend_rom_36
   cmp_rd_data
   command_logic
   data_tap_inc
   idelay_ctrl
      idelay_rd_en
   rd_data_fifo
   tap_ctrl
   v4_dm_iob
   v4_dq_iob
   V4_dqs_iob
```

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/10/04	1.0	Initial Xilinx release.
11/16/04	1.1	Revised “ACTIVE Command” and “Write Command” sections. Added a link to the reference design. Completed Table 3.