Achieving Breakthrough Performance with Virtex-4, the World’s Fastest FPGA

Xilinx 90nm Design Seminar Series:
Part I

Xilinx - #1 in 90 nm
We Asked our Customers:

*What are your challenges?*

- Shorter design time, faster obsolescence
- More competition, increasing cost pressure
- Demanding complexity and performance,
- Signal integrity problems caused by faster I/O
- Power consumption and thermal issues

- Today’s seminar addresses *Performance*
90 nm Technology

• Proof that Moore’s “Law” is still alive
  — “Every two years, twice the number of transistors”
  — Every five years, twice the speed
  — Half the size = 2x chips/wafer = half the cost,
  — Smaller distances = less capacitance = higher speed
  — Less C and lower V = less dynamic power = fCV^2

• Xilinx has extensive design and manufacturing experience
  — Spartan-3™ since 2003, Virtex-4™ since mid-2004

Xilinx has shipped 100 times more 90nm devices than all other FPGA manufacturers combined
500 MHz Virtex-4...

1. 90 nm *technology* is the foundation
   - More transistors, faster speed and lower cost
2. Clever *circuit design* builds on that foundation
   - Smaller size, lower power, and higher performance
3. *Architectural innovation*, novel features
   - Hard-coded IP:
     - PowerPC®, BRAM-FIFO, DSP-MAC
     - Source-synchronous I/O with delay-line on every pin,
     - Dedicated Multi-Gigabit Transceivers up to 10 Gbps
4. Continuously improving design tools, easier to use

...the fastest FPGA family in the world
Architectural Innovation

- 500 MHz Logic Array
- 500 MHz Differential Clocking
- >1 Gbps diff I/O with ChipSync™
- 500 MHz PowerPC with APU
- 450 MHz PowerPC with APU
- 500 MHz XtremeDSP Slice
- 500 MHz BRAM and FIFO
- 622 Mbps to over 10 Gbps RocketIO
Virtex-4: Highest FPGA Performance

- I/O LVDS Bandwidth: 480 Gbps
- I/O Memory Bandwidth: 260 Gbps
- High-speed Serial I/O: 10 Gbps
- On-chip RAM Speed: 500 MHz
- DSP: 32-Tap Filter: 702 DMIPS
- Logic Fabric Performance: Benchmark

Breakthrough Performance
Better Functions = Higher Speed

The biggest performance boost comes from:

• Versatile clocking
• Parallel I/O and memory interfaces
• Serial I/O, multi-gigabit transceivers
• Memory (distributed RAM, BlockRAM, FIFOs)
• Expandable DSP slices
• Fast synchronous counters
• Embedded processing
• Fabric logic resources and interconnect structure

*Functionality can triple the performance*
Architectural Innovation

- 500 MHz Logic Array
- 450 MHz PowerPC with APU
- 500 MHz XtremeDSP Slice
- 500 MHz BRAM and FIFO

500 MHz Differential Clocking

>1 Gbps diff I/O with ChipSync™

622 Mbps to over 10 Gbps RocketIO
Versatile Clocking

• 32 Global clock lines can cover the whole chip
  — Fast rise and fall times, low skew, differential
  — Optimal for DDR operation, avoids duty-cycle distortion
    (skew, transition time and distortion would lower design margins)

• Distributed local clocks:
  — Regional clocks avoid the need for slow clock routing
  — Very fast I/O clocks, up to 500 MHz = 1Gbps

Rugged clocks, the backbone of any design
Precise Clock Management

• Phase-aligned frequency control

• **Eliminates** on-chip clock delay
  — Of vital importance on larger chips
  — Can also eliminate PC-board clock delay

• **Simultaneous** multiplication and division
  — Frequency synthesis

• Dynamic Clock Phase adjust (servo-controlled)
  in 256 steps with 50 ps granularity

*Picosecond precision and granularity*
Architectural Innovation

500 MHz Logic Array

500 MHz Differential Clocking

>1 Gbps diff I/O with ChipSync™

500 MHz BRAM and FIFO

500 MHz XtremeDSP Slice

450 MHz PowerPC with APU

622 Mbps to over 10 Gbps RocketIO
High-Speed Inputs and Outputs

- Traditional **System-Synchronous** @ <200 MHz
  - One central clock arrives everywhere “simultaneously”
- **Source-Synchronous** Clocking @ >200 MHz
  - A dedicated clock always travels with the data
  - Avoids all PC-board delay issues
  - Receiver must precision-align clock or strobe with the data eye

*I/O data rate often exceeds internal data rate*
Parallel I/O

Optimized for Source-Synchronous Interfaces
• Programmable precision delay on every input pin
  — Can align data to strobe or clock, or compensate pc board
• Serial-to-parallel converter on every input pin
• Parallel-to-serial converter on every output pin
  — Does not rely on global clocks

Speed and Bandwidth
• Networking Interfaces: 1+ Gbps differential
• Memory Interfaces: 600 Mbps single ended

All I/O pins are created equal
Precise Timing Adjustment

Independent IDELAY on every input pin
Automatic calibration with 64 taps of 78 ps each
ChipSync Precision Timing

- **ChipSync IDELAY**
  - Automatically aligns data and clock
  - 78 ps resolution for precise clock-to-data centering
  - Increases design margins for higher system reliability

*Not available in any other FPGA, ASIC or ASSP*
1 Gbps S/P on Every Input Pin

- Serial-to-Parallel Converter on every input pin
  - Frequency division by 2, 3, 4, 5, 6, 7, 8 or 10
- Works in conjunction with IDELAY block
  - Dynamic signal alignment for bit, word, or clock
  - Supports Dynamic Phase Alignment (DPA)

Requires no resources in the fabric
1 Gbps P/S on Every Output Pin

- Parallel-to-Serial Converter on every output pin
  - Frequency multiplication by 2, 3, 4, 5, 6, 7, 8 or 10

Requires no resources in the fabric
Wide Memory Interfaces

- Source-synchronous for highest performance
- All Virtex-4 pins have the same capabilities
  - Wide memory interfaces on all 4 sides
  - Highest bandwidth, up to 432 bits @ 600 Mbps DDR

- Evaluation board demonstrates interfaces to:
  - DDR, DDR2, QDR-II SRAM, RLDRAM-II, FCRAM-II

Supported by multi-standard evaluation board ML461
ML461 Advanced Memory Development System

Available Now

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ML450 Source Synchronous I/F Development System

Available Now

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<th>Standards</th>
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<td>Utopia IV</td>
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RocketIO™ transceivers
— Full-duplex w/ integrated SERDES, FIFOs, and CDR
— 8-24 channels per chip, Data rate: 622Mbps-10Gbps
— Transmit pre-emphasis, receive equalization

Fastest I/O in any FPGA
Architectural Innovation

500 MHz Logic Array

500 MHz Differential Clocking

>1 Gbps diff I/O with ChipSync™

500 MHz BRAM and FIFO

500 MHz XtremeDSP Slice

450 MHz PowerPC with APU

622 Mbps to over 10 Gbps RocketIO
DSP Building Block

• FPGAs do high-performance DSP extremely well
  – Thanks to massive parallelism (500+ engines)
  – Fast clock rate, pipelined, high throughput
• Needs many fast Multiplier-Accumulators (MACs)
  – Dedicated, repetitive (systolic) structure
  – Slightly programmable, must be expandable

Can be the fastest DSP, if done right…
Traditional DSP Algorithm Implementation, 32-Tap FIR Filter

- 4-deep MAC blocks need fabric support
- Cascaded adder tree becomes the performance bottleneck

Example: 32-tap FIR Filter

- 235.7 MHz in Slow grade
- 347.9 MHz in Fast grade

*When you are fast, every single nanosecond hurts*
Unbeatable DSP Performance

ASMBL advantage:

- Cascade throughout vertical column without any help from the fabric
- Speed not affected by external adder tree
- 57% faster than the traditional approach

Example:
Systolic 32-tap FIR Filter

- 400 MHz in Slow grade
- 500 MHz in Fast grade
Expansion Without Extra Logic...

- 500 MHz unlimited pipelined cascade
- No ripple delay for any filter size

32-tap FIR filter runs at 500 MHz
Uses 32 DSP Slices and no resources in the fabric
Expandable DSP Slice (MAC)

- BCOUT (18-bit)
- PCOUT (48-bit)
- BCIN (18-bit)
- PCIN (48-bit)
- A (18-bit)
- B (18-bit)
- C (48-bit)
- P (48-bit)

500 MHz

Optional Pipeline Register, Routing Logic
Multiplier, Optional Register
Optional Pipeline Register, Routing Logic
Virtex-4 MUX Solution

- Six-to-one: 36-bit-wide MUX in only 4 DSP Slices
- Five-to-one: 36-bit-wide MUX in only 3 DSP Slices
- Two-level pipeline assures 500 MHz performance

Innovative use of DSP slices, “not just for filters”
...+ other Applications

Counters:

- 32-bit synchronous loadable counter @ 500 MHz or
  - in 1 slice (high speed thanks to smart carry structure)
- 48-bit synchronous non-loadable counter @ 500 MHz

- 18-bit Barrel shifter, using the multiplier

- 32-bit Direct Digital Synthesis @ 500 MHz
  - Phase accumulator can achieve virtual 8 GHz operation
    with the help of one BlockRAM and 16 IDELAYs

Each chip has between 32 and 512 such DSP slices
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500 MHz Differential Clocking

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450 MHz PowerPC with APU

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500 MHz BRAM and FIFO

622 Mbps to over 10 Gbps RocketIO

Architectural Innovation
Fast 18Kb-BlockRAM

- Pipelined 500MHz synchronous operation
- Width-adjustable per port
- Read before write, or write before read
- Built-in FIFO controller in each BlockRAM
- Built-in Hamming error correction for 64 bits

Ideal for
- Microprocessor data / instructions and fast state machines

48 to 552 BlockRAMs per chip
Fast State Machine

- 256 states, 4-way branch, **350 MHz guaranteed**
  - or 128 states, 8-way branch, same speed
  - or 64 states, 16-way branch, same speed
...plus 36 More Outputs

- 36 additional parallel outputs
  —from the other half of the BlockRAM
...and Many Control Inputs

- 64, 128, or 256 states with multi-branch capability
- 36 freely assigned + 8 encoded outputs
- Optional multiplexed control inputs

All in one BlockRAM plus 2 CLBs
Dual-Clock FIFO

Conceptually very simple:
• Use dual-port RAM + two counters + comparators

Problem:
• Decoding FULL and EMPTY when using unrelated clocks for write and read
  — Requires Gray-coded counters
  — Complicates partial full/empty decoding
• Synchronize EMPTY flag to read clock
• Trailing edge causes metastability concerns

Requires good understanding of asynchronous issues
500 MHz Dual-Clock FIFO

- A FIFO controller in every Virtex-4 BlockRAM
  - Tested at 500 MHz with $10^{14}$ flag cycles

- Testing details:
  - Write at 200 MHz, read asynchr. at 500 MHz
  - Goes EMPTY after every write, stops reading
  - 200 M asynchronous arbitrations per second
  - No errors for $10^{14}$ cycles

- Don’t worry about metastability, we did it for you!

Complete solution in every Virtex-4 BlockRAM FIFO
Architectural Innovation

- 500 MHz Logic Array
- 500 MHz Differential Clocking
- >1 Gbps diff I/O with ChipSync™
- 500 MHz BRAM and FIFO
- 500 MHz XtremeDSP Slice
- 500 MHz PowerPC with APU
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Embedded Microprocessors

- Many designs combine fast logic and arithmetic with much slower functions.
- Fast logic is executed in the fabric “nanosecond logic”
- Slower, but more complex functions are best executed by μP or μController “microsecond or millisecond logic”

*Slow functions benefit from μP design flexibility*
Soft Microprocessor Cores

- Soft processors use fabric + BlockRAMs
  - PicoBlaze, MicroBlaze
- Flexible and versatile, but more limited than a hard µP like PowerPC
- Soft µPs use 100 to 1K slices plus RAMs
  - MHz clock speed and up to 200 DMIPS

*Soft processors for simple and slow tasks*
Highest-Performance FPGA Microprocessor

• High-performance PowerPC Core
  – Up to two cores per Virtex-4 FX device
  – 702 DMIPS per core
  – Integrated 16Kbyte Instruction Cache
  – Integrated 16Kbyte Data Cache

• Acceleration through Auxiliary Processor Unit (APU) Interface
  – Provides direct access from FPGA fabric to PowerPC core
  – High-performance coprocessor support

More than 3 times faster than any soft µP
Architectural Innovation

500 MHz Logic Array

500 MHz Differential Clocking

>1 Gbps diff I/O with ChipSync™

500 MHz BRAM and FIFO

Virtex X4

500 MHz XtremeDSP Slice

450 MHz PowerPC with APU

622 Mbps to over 10 Gbps RocketIO
Fabric Resources

1 CLB = 4 Slices = 8 VLUTs
• Variable Look-Up-Table for:
  – Logic of 4, 5, 6 or 7 inputs
  – Distributed memory
  – 16-bit shift register, SRL16
• No shared inputs
  – Can pack unrelated functions
• Eight Flip-flops per CLB
• Fast carry

Logic and routing support 500 MHz operation
Benchmarks Should Guide and Help the User

- Meaningful and realistic benchmarks must:
  - Compare equivalent speed grades
  - Use the best available software options
  - Constrain both synthesis and place and route
  - Use meaningful design examples
  - Evaluate real functions, not just LUTs
  - Utilize available embedded functions
Benchmarks Should Guide and Help the User

"We agree that Xilinx' constraint-based benchmarking methodology delivers a robust and accurate assessment of device performance for a broad variety of real-world customer designs."

"This methodology for measuring performance has enabled us to tune Synplify Pro to achieve continuously superior results for Xilinx devices. With the new version of the Synplify Pro software and the Xilinx ISE Software, Synplicity and Xilinx continue to offer the industry great results."

Ken McElvain, CTO, Synplicity
Benchmarks to Measure Fabric Performance

Virtex-4 FPGAs

90nm Competitor

Logic performance testing of fastest speed grades using real customer designs and the best available tools

Average: 15% advantage
Performance is not Determined by Traditional Benchmarks Alone

• Old designs obviously are not optimized for the new architectural features

• Performance should be measured as a composite of typical system requirements:
  – Fabric, I/O, on-chip memory, memory interfaces, DSP, embedded processing, etc.
Virtex-4 Leads in 7 of 7 Performance Criteria

<table>
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<th>Xilinx Virtex-4™ FPGAs</th>
<th>90 nm competitor</th>
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<tbody>
<tr>
<td>I/O LVDS Bandwidth</td>
<td>1.6x</td>
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<tr>
<td>I/O Memory Bandwidth</td>
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<td>High-speed Serial I/O</td>
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<td>On-chip RAM</td>
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<tr>
<td>DSP: 32-Tap Filter</td>
<td>3x</td>
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<td>Embedded Processing</td>
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<td>Logic Fabric</td>
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Data based on competitor’s published datasheet numbers

Performance up to 3x higher than competing FPGAs
Summary

• Xilinx is First in 90nm FPGAs
  – 100x more devices shipped than by all other PLD vendors combined

• Virtex-4 is the world’s fastest FPGA
  – Traditional benchmarks show performance advantage in fabric
  – New functions enable breakthrough performance + reduced power + lower cost

Virtex-4 : Product of the Year
"…a boost in speed, reduction in power, and significant reduction in cost…"