

PS/2 Encoder/Decoder

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1.0 About this design

The PS/2 encoder/decoder described in this project can be used to receive information from and send commands to a PS/2 device. The device uses the LED display to display codes received by the device. An internal register queue is used to buffer up to 16 codes and display them in a first in first out order for approximately 1 second each. Single control codes can also be sent to the device when required. This project requires a 1MHz input clock to operate.

2.0 Files needed for this design

List of Files

- hdps2key.vhd
- siposhiftreg.vhd
- pisoshiftreg.vhd
- switchpause.vhd
- clockpause.vhd
- seg7.vhd
- parity.vhd
- registerfile.vhd
- reader.vhd
- ps2dcd.vhd
- dwnldhex.vhd
- ps2pins.ucf
- dwnldhexpins.ucf

File Descriptions

hdps2key.vhd

Top level file which connects all the devices used in this project together and converts outputs for display on the LEDs etc.

siposhiftreg.vhd

Implements a SIPO shift register which shifts right, shifting into the MSB.

pisoshiftreg.vhd

Parallel in / serial out shift register which shifts right, shifting out the LSB

switchpause.vhd

Debounces the input switch so that multiple writes are not performed to the device. Once asserted, the output will not assert again until about a second has passed.

clockpause.vhd

Creates a delay of 64 clock cycles for the PS/2 signal.

seg7.vhd

Convert binary input data into a digit on the 7-segment display.

parity.vhd

Manages the parity bit of the PS/2 device

registerfile.vhd

A register queue storing up to 16 bytes of data to be shifted out on request. This operates on a first in, first out basis.

reader.vhd

Displays information in the register file queue at 1 byte per second. Starts reading as soon as there is data in the queue , and will continue to read until the queue is empty.

ps2dcd.vhd

State machine which converts serial data from the PS/2 device into bytes and adds them to the queue. Also controls the sending of information to the PS/2 device.

dwnldhex.vhd

File that should be compiled into an SVF for the CPLD. This disables the parallel port once the download is complete so that the LED display may be used by the FPGA without contention.

ps2pins.ucf

UCF file containing pin locations for the ps/2 encoder/decoder design.

dwnldhexpins.ucf

UCF file containing pin locations for the CPLD file.

3.0 Description of the design

Using the project

This project requires the on-board oscillator to be running at 1MHz. To use the project, connect a PS/2 keyboard or mouse to the board and download the bit file. Any bytes received by the decoder will be added to the queue and start displaying immediately. To send bytes to the device, put the byte data onto the 8 dipswitches with switch 8 as the least significant bit and press push button 4 to send. Data can only be sent about once per second due to the debouncing technique used on the switch.

Ways to use project

To use a PS/2 keyboard, press and release a key on the keyboard and you should see the scan codes for the data displayed sequentially on the hex display. You can also send commands to change the status of the lock LEDs (Caps Lock etc.) on the keyboard on or off. For more information see <http://govschl.ndsu.nodak.edu/~achapwes/PICmicro/PS2/ps2.htm> or other PS/2 protocol description sources. PS/2 mice can be connected as well, but require codes to be sent to them before they will reply with any data.

Modules

Many of the vhdl files used in this project can be used separately due to the way it was coded. Files such as the parity generator and shift registers could easily be used in other projects, but they would be better off included in the state machines that use them instead. The PS/2 decoder file can be used without the register file, switch pause, reader and seg7 files as a plug-in to read and write to a keyboard or mouse. This would eliminate all the 1 second delays and can be used by another on-chip project as an input device. The additional files are added simply to make an easily testable human interface.

Extensions

As long as the clock pause.vhd file is changed to handle it, a much faster clock can also be used in this project. It should be able to handle any speed higher than 1MHz. The clockpause.vhd file must still generate a pause of at least 60us. Most of the files used, such as parity and the counter should be moved into the VHDL file of the decoder. There is no real reason for them to be separate, and they increase the number of files in the project for no reason.