MOS Transistors as Switches

\[ G \quad (\text{gate}) \]
\[ D \quad (\text{drain}) \]
\[ S \quad (\text{source}) \]

**nMOS transistor:**
- Closed (conducting) when Gate = 1 (Vdd, 5V)
- Open (non-conducting) when Gate = 0 (ground, 0V)

**pMOS transistor:**
- Closed (conducting) when Gate = 0 (ground, 0V)
- Open (non-conducting) when Gate = 1 (Vdd, 5V)

For \textit{nMOS} switch, source is typically tied to ground and is used to \textit{pull-down} signals:

\[ G \]
\[ S \]
\[ \text{Out} \]

when Gate = 1, Out = 0, (OV)

when Gate = 0, Out = Z (high impedance)

For \textit{pMOS} switch, source is typically tied to Vdd, used to \textit{pull} signals \textit{up}:

\[ G \]
\[ S \]
\[ \text{Out} \]

when Gate = 0, Out = 1 (Vdd)

when Gate = 1, Out = Z (high impedance)

Note: The MOS transistor is a symmetric device. This means that the drain and source terminals are interchangeable. For a conducting \textit{nMOS} transistor, \( V_{DS} > 0V \); for the \textit{pMOS} transistor, \( V_{DS} < 0V \) (or \( V_{SD} > 0V \)).
The CMOS Inverter

Note: Ideally there is no static power dissipation. When "I" is fully high or fully low, no current path between Vdd and GND exists (the output is usually tied to the gate of another MOS transistor which has a very high input impedance).

Power is dissipated as "I" transitions from 0 → 1 and 1 → 0 and a momentary current path exists between Vdd and GND. Power is also dissipated in the charging and discharging of gate capacitances.
Parallel Connection of Switches

\[ Y = 0, \text{ if } A \text{ or } B = 1 \]

\[ A + B \]

\[ Y = 1, \text{ if } A \text{ or } B = 0 \]

\[ \overline{A} + \overline{B} \]

Series Connection of Switches

\[ Y = 0, \text{ if } A \text{ and } B = 1 \]

\[ A \cdot B \]

\[ Y = 1, \text{ if } A \text{ and } B = 0 \]

\[ \overline{A} \cdot \overline{B} \]
NAND Gate Design

*p*-type transistor tree will provide "1" values of logic function

*n*-type transistor tree will provide "0" values of logic function

Truth Table (NAND):

<table>
<thead>
<tr>
<th>AB</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>1</td>
</tr>
<tr>
<td>01</td>
<td>1</td>
</tr>
<tr>
<td>10</td>
<td>1</td>
</tr>
<tr>
<td>11</td>
<td>0</td>
</tr>
</tbody>
</table>

K-map (NAND):

```
+---+---+
|   |   |   |
| 1 | 1 |   |
| 1 | 1 | 0 |
+---+---+
```

NAND circuit example:

\[ P_{\text{tree}} = \overline{A} + \overline{B} \]
\[ N_{\text{tree}} = A \cdot B \]
NOR Gate Design

$p$-type transistor tree will provide "1" values of logic function
$n$-type transistor tree will provide "0" values of logic function

Truth Table:

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K-map:

NOR circuit example:

\[ P_{\text{tree}} = \overline{A} \cdot \overline{B} \]
\[ N_{\text{tree}} = A + B \]
What logic gate is this?

\[ Y = \begin{cases} 1 & \text{when } A \cdot B \\ 0 & \text{when } \overline{A} + \overline{B} \end{cases} \]

Answer: AND function, but poor design!

Why? nMOS switches cannot pass a logic "1" without a threshold voltage (\(V_T\)) drop.

\[ V_{DD} \quad G \quad V_{DD} \quad G \quad V_{DD} - V_T \]

where \(V_T = 0.7V\) to \(1.0V\) (i.e.,

threshold voltage will vary)

output voltage = 4.3V to 4.0V,

a weak "1"
The $n$MOS transistor will stop conducting if $V_{GS} < V_T$. Let $V_T = 0.7V$,

![Diagram of MOS transistor with 5V source and 0V drain, showing 0V to 5V and 0V to ?]

As source goes from 0V → 5V, $V_{GS}$ goes from 5V → 0V.
When $V_S > 4.3V$, then $V_{GS} < V_T$, so switch stops conducting.
$V_D$ left at $5V - V_T = 5V - 0.7V = 4.3V$ or $V_{dd} - V_T$.

What about $n$MOS in series?

![Diagram of series of MOS transistors with 5V and 4.3V voltages, showing 0V to 5V, 0V to 4.3V, 0V to 4.3V, 0V to 4.3V, and 0V to $V_{dd} - V_T$ with 5V - 0.7V and 4.3V labels]

Only one threshold voltage drop across series of $n$MOS transistors
For pMOS transistor, $V_T$ is negative.

pMOS transistor will conduct if $|V_{GS}| > |V_{TP}|$ ($V_{SG} > |V_{TP}|$),

or $V_{GS} < V_{TP}$

\[
\begin{array}{c}
0V \\
G \\
\hline \\
5V \\
S \\
\hline \\
D \\
\end{array}
\]

$V_{TP} = -0.7V$

$V_{GS} = 0V - 5V = -5V$

conducting

$V_{GS} < V_{TP}$ or $|V_{GS}| > |V_{TP}|$

$-5V < -0.7V$ $5V > 0.7V$

How will pMOS pass a "0"?

When $|V_{GS}| < |V_{TP}|$, stop conducting

\[
\begin{array}{c}
G \\
\hline \\
0V \\
\end{array}
\]

\[
\begin{array}{c}
5V \\
S \rightarrow D \\
\hline \\
5V \rightarrow ? \\
D \rightarrow ? \\
\end{array}
\]

So when $|V_{GS}| < |-0.7V|$, $V_D$ will go from $5V \rightarrow 0.7V$,

a weak "0"

How are both a strong "1" and a strong "0" passed?

Transmission gate pass transistor configuration

When $I = 1$, $B = \text{strong 1, if } A = 1$;

$B = \text{strong 0, if } A = 0$

When $I = 0$, non-conducting
About that AND Gate...

No!!!
Poorly designed AND
(circuit designer fired)

Instead use this,