Combinational Building Blocks

2/1 Multiplexor (MUX)

\[ I_0 \quad Y \quad I_1 \quad S \]

- If \( S = 0 \), then \( Y = I_0 \)
- If \( S = 1 \), then \( Y = I_1 \)

\[ Y = I_0 \, S' + I_1 \, S \]


D[3:0]  S

Muxes often use to select groups of bits arranged in buses.

What Good are Muxes ??

Sometimes want to have a bus be driven from multiple blocks, where only one block is driving the bus at a time.

Logic A  10  Y  4/1 Mux
Logic B  11
Logic C  12
Logic D  13  S[1:0]

N to 1 mux will select 1 source; Select bus needs to be \( \log_2(N) \). Note that only ONE input can be selected at a time!

Higher Order Muxes

4/1 Mux

\[ I_0 \quad Y \quad I_1 \quad I_2 \quad I_3 \quad S[1:0] \]

- If \( S = "00" \), then \( Y = I_0 \)
- If \( S = "01" \), then \( Y = I_1 \)
- If \( S = "10" \), then \( Y = I_2 \)
- If \( S = "11" \), then \( Y = I_3 \)

\[ Y = I_0 \, S_1' \, S_0' + I_1 \, S_1' \, S_0 + I_2 \, S_1 \, S_0' + I_3 \, S_1 \, S_0 \]

8/1 Mux

\[ I_0 \quad I_1 \quad I_2 \quad I_3 \quad I_4 \quad I_5 \quad I_6 \quad I_7 \quad S[2:0] \]

\[ Y \]

- If \( S = 000 \), then \( Y = I_0 \)
- If \( S = 001 \), then \( Y = I_1 \)
- If \( S = 010 \), then \( Y = I_2 \)
- If \( S = 011 \), then \( Y = I_3 \)
- If \( S = 100 \), then \( Y = I_4 \)
- If \( S = 101 \), then \( Y = I_5 \)
- If \( S = 110 \), then \( Y = I_6 \)
- If \( S = 111 \), then \( Y = I_7 \)

\[ Y = I_0 \, S_2' \, S_1' \, S_0' + I_1 \, S_2' \, S_1' \, S_0 + I_2 \, S_2 \, S_1' \, S_0' + I_3 \, S_2 \, S_1' \, S_0 + I_4 \, S_2 \, S_1 \, S_0' + I_5 \, S_2 \, S_1 \, S_0 + I_6 \, S_2' \, S_1 \, S_0 + I_7 \, S_2 \, S_1 \, S_0 \]
Logic for 2/1, 4/1 Muxes

\[ Y = I_0 S' + I_1 S \]

\[ Y = I_0 S_1' S_0' + I_1 S_1' S_0 + I_2 S_1 S_0' + I_3 S_1 S_0 \]

These are called COMBINATIONAL muxes.

Tri State Buffer

There is another way to drive a line or bus from multiple sources. Use a TRISTATE buffer.

When EN = 1, then \( Y = A \).

When EN = 0, then \( Y = \text{??????} \)

Y is undriven, this is called the high impedance state.

Designate high impedance by a ‘Z’.

When EN = 0, then \( Y = 'Z' \) (high impedance)

Using TriState Buffers

Can use tristate buffers instead of a combinational 2/1 mux

EN_A

EN_B

Y

Must make sure that EN_A, EN_B are not both ‘1’ at same time, or Y will be driven from multiple sources
Using TriState Buffers (cont)

Only A or B is enabled at a time.

![Diagram 1]

Implements 2/1 Mux function

If S=0 then Y = A
If S=1 then Y = B

Using TriState Buffers (cont)

Y is driven by A, B, C or D; only one source is enabled at a time.

![Diagram 2]

Implements 4/1 MUX function.

Decoders

Logic common to both of the previous mux implementations was the decoder function.

1 to 2 decoder

S

Y0 = S'
Y1 = S

2 to 4 decoder

S[1:0]

Y0 = S1'S0'
Y1 = S1'S0
Y2 = S1'S0'
Y3 = SIS0
### Logic for 4/1 Combinational Mux

- Inputs: $Y_0, Y_1, Y_2, Y_3$
- Select inputs: $S[1:0]$
- Outputs: $Y$

#### 2 to 4 decoder

### 4/1 Mux using Decoder + TSBs

- Inputs: $Y_0, Y_1, Y_2, Y_3$
- Select inputs: $S[1:0]$
- Outputs: $Y$

#### 2 to 4 decoder

### 3 to 8 Decoder

- Inputs: $A[2:0]$
- Outputs: $Y_0, Y_1, Y_2, Y_3, Y_4, Y_5, Y_6, Y_7$

#### 2 to 4 decoder
N-Bit Wide Elements

To build a 2/1 mux for 4-bit wide buses, need four 1-bit 2/1 muxes.

Review of Memory example

F (A,B,C) = A \oplus B \oplus C  \quad G = AB + AC + BC

Recall that Exclusive OR (\oplus) is

Y = A \oplus B

Location 0 has “00”,
Location 1 has “10”,
Location 2 has “10”, etc....

Binary Adder

F (A,B,C) = A \oplus B \oplus C  \quad G = AB + AC + BC

These equations look familiar. These define a Binary Full Adder:

Sum = A \oplus B \oplus Cin
Cout = AB + Cin A + Cin B
     = AB + Cin (A + B)
4 Bit Ripple Carry Adder

Incrementer

What do You have to know?

• Structures for Muxes, Decoders, Ripple Carry adder, Incrementer
• What a tristate buffer is
• How to build muxes from all combinational logic or from combinational logic + tristate buffers
• Bus naming convention
• How to build N-bit wide elements from 1-bit wide elements