FSM Timing Examples

What does timing look like?

Timing

How is this different?
Timing

CLK
State
S0 S1 ?? ?? ??
Start
Inc_cnt
S00 S01 S02
Q
1st edge after Start, Cntr=0; 2nd edge Cntr=1

Checking for End of Count

Inc_cnt = 1
Cntr=F?
0
S3 S4
F S M Inc_cnt C N T R Q[3..0]
4 bit counter

Final value of 4-bit counter is 0.

What does timing look like?
How is this different?

How is this different?

Timing

Register, FSM uses rising edge DFFs

Another example of FSM timing, this time controlling a register.

State

Inc_cnt

Q

S3

S4

Final value of 4-bit counter is F.

What value does register end up with considering the following ASM charts?
A Comparator

Another common combinational building block is a comparator.

A \equiv B \text{ if } A(i) = B(i) \text{ and } A(1) = B(1) \text{ and } \dots \text{ and } A(n-1) = B(n-1)

Recall that "\text{xnor}" function is '1' if \( A = 0 \), \( B = 0 \) or \( A = 1 \), \( B = 1 \)! So \( \text{A} \equiv \text{B} \) is:

\[ \text{A} \equiv \text{B} = (A(0) \text{xnor } B(0)) \text{ and } (A(1) \text{xnor } B(1)) \text{ and } \ldots \text{etc.} \]
FSM/Datapaths No-Nos

Control of asynchronous clear by FSM - bad!!
Glitch on aclr line by FSM logic can cause inadvertent clear operation! Also, generally want synchronous behavior of CNTR during FSM operation (all outputs changing on clock edges).

Control of synchronous clear by FSM. Good!

1 Bit Register with Synchronous Clear

Note that SCLR = 1 will set DFF=0 on next active clock edge.

Register Timing (8 Bit register)

Glitch on SCLR, no effect.
Glitch on ACLR, clears register.
What Causes Glitches on outputs of FSMs?

- Many combinational paths in logic that defines next state.
- If these paths have unequal numbers of gates, or gates have different delays, then glitches can occur.
- We normally don’t care about these glitches as long as the output lines are STABLE before the next clock edge (satisfy the setup time requirement)
- If output lines are connected to asynchronous control inputs, then glitches can be a BIG problem!
- Solution: Don’t connect asynchronous controls lines to FSM outputs or guarantee FSM outputs are glitch free (come directly from a FF).

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FSM/Datapaths No-Nos

This datapath is trying to accumulate a multiply/add from data values in registers RA, RB, RC.

The adder has a COMBINATIONAL LOOP!! Will oscillate!!! Bad!!!

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FSM/Datapaths No-Nos

Must use a Register to hold value of multiply/add for next multiply/add operation. Good!!!