Work all problems.

1. (5 pts) Identify the following device. What values do the inputs have to be for the outputs to have the following values \( Y_0 = 0, Y_1 = 0, Y_2 = 1, Y_3 = 0 \).

2. (8 pts) Assume that the initial state device shown below is a '0'. Draw a timing diagram that will cause the state of the device to be changed to '1'.

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SSN: ______________________ (no names please)
3. (8 pts) Complete the timing diagram below for the Q output of the device that is shown.

```
D
Q
G
```

```
G
```

```
D
```

```
Q
```

4. (8 pts) Complete the timing diagram below for the Q output of the device that is shown.

```
D
Q
C
```

```
C
```

```
D
```

```
Q
```
5. (8 pts) Complete the timing diagram below for the Q output of the device that is shown.

![Timing Diagram](image)

6. For a flip-flop of your choosing (D, J-K, T), draw a timing diagram and illustrate setup and hold time constraints.

7. (5 pts) What is the clock period of a 50 MHz clock (1 MHz = 10^6)
8. (5 pts) What is the value of $A3$ shifted to the right by one position with the serial input bit = ‘1’?

9. (5 pts) How is an asynchronous input different from a synchronous input?

10. Draw the schematic for a 1-bit register. The inputs are CLK, D, LD. The output is Q. The LD input is high true.

11. Draw the diagram of a rising edge triggered D-FF using D Latches.
12. (10 pts) Draw a schematic for a 3-bit counter that has a parallel load. Use a three bit incrementer combinational logic block as one of your building blocks (the incrementer has a 3-bit input A[2..0], a one bit input EN, a three bit output Y[2..0]. When EN=1, then Y = A+1; when EN=0, then Y=A). The inputs to the counter is CLK, DIN[2..0], LD, EN. The output is DOUT[2..0]. The LD, EN inputs are high true. (You do not have to show the internals of the incrementer block).

13. (10 pts) Draw the schematic of a 4-1 mux using Tri-state buffers. You can use an decoder block in your design, and you do not have to show the internal details of the decoder.