Programmable Logic

- So far, have only talked about PALs (see 22V10 figure next page).
- What is the next step in the evolution of PLDs?
  - More gates!
- How do we get more gates? We could put several PALs on one chip and put an interconnection matrix between them!!
  - This is called a Complex PLD (CPLD).

Any other approaches?

Another approach to building a “better” PLD is place a lot of primitive gates on a die, and then place programmable interconnect between them:

Field Programmable Gate Arrays

The FPGA approach to arrange primitive logic elements (logic cells) arrange in rows/columns with programmable routing between them.

What constitutes a primitive logic element? Lots of different choices can be made! Primitive element must be classified as a “complete logic family”:

- A primitive gate like a NAND gate
- A 2/1 mux (this happens to be a complete logic family)
- A Lookup table (i.e., 16x1 lookup table can implement any 4 input logic function).

Often combine one of the above with a DFF to form the primitive logic element.

Other FPGA features

- Besides primitive logic elements and programmable routing, some FPGA families add other features
- Embedded memory
  - Many hardware applications need memory for data storage. Many FPGAs include blocks of RAM for this purpose
- Dedicated logic for carry generation, or other arithmetic functions
- Phase locked loops for clock synchronization, division, multiplication.
Altera Flex 10K FPGA Family

Table 1. FLEX 10K Device Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>EPF10K10</th>
<th>EPF10K20</th>
<th>EPF10K30</th>
<th>EPF10K40</th>
<th>EPF10K50</th>
<th>EPF10K50V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical gates (logic and RAM), Note 1</td>
<td>10,000</td>
<td>20,000</td>
<td>30,000</td>
<td>40,000</td>
<td>50,000</td>
<td></td>
</tr>
<tr>
<td>Usable gates</td>
<td>7,000 to</td>
<td>15,000 to</td>
<td>22,000 to</td>
<td>28,000 to</td>
<td>36,000 to</td>
<td>44,000 to</td>
</tr>
<tr>
<td>Logic elements (LEs)</td>
<td>576</td>
<td>1,152</td>
<td>1,728</td>
<td>2,304</td>
<td>2,880</td>
<td>3,456</td>
</tr>
<tr>
<td>Logic array blocks (LABs)</td>
<td>72</td>
<td>144</td>
<td>216</td>
<td>288</td>
<td>360</td>
<td></td>
</tr>
<tr>
<td>Embedded array blocks (EABs)</td>
<td>3</td>
<td>6</td>
<td>6</td>
<td>8</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Total RAM bits</td>
<td>6,144</td>
<td>12,288</td>
<td>12,288</td>
<td>10,384</td>
<td>20,480</td>
<td></td>
</tr>
<tr>
<td>Maximum user I/O pins</td>
<td>134</td>
<td>248</td>
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<td></td>
</tr>
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Note to table:
(1) For designs that require 1LE boundary scanning, the total LE count is 2% less than the LE count shown above.

Altera Flex 10K FPGA Family (cont)

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Dedicated memory

Figure 1. FLEX 10K Device Block Diagram

Figure 6. FLEX 10K Logic Element

16 x 1 LUT

Embedded Array Block

• Memory block, Can be configured:
  – 256 x 8, 512 x 4, 1024 x 2, 2048 x 1

Figure 3. Examples of Combining LABs

Figure 5. FLEX 10K LAB

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Altera APEX II
- Altera’s latest FPGA family is the APEX II
- Latest addition is support for high speed serial transfer protocols, embedded processor cores

Differential Serial IO support in APEX II
- Separate PLL for differential receivers
- 1 Gbps per receiver

Altera Excalibur device has embedded processor + programmable logic.

Altera NIOS processor IP block
- An IP (Intellectual Property) block is some functional block such as a PCI bus interface, processor, etc specified in an RTL and mapped to an FPGA implementation
  - Altera licenses IP based on their FPGAs so companies do not have to re-invent the wheel
- NIOS softcore processor specs:
  - Load/store RISC architecture
  - Datapath size of 16 or 32 bits
  - 16 bit instruction set
  - 5 stage pipeline
  - Up to 512 registers (windowed, 32 visible)
  - 13% of Apex 20K200 device (16 bit datapath), 20% in 32-bit datapath configuration
  - User can add custom instructions

Issues in FPGA Technologies
- Complexity of Logic Element
  - How many inputs/outputs for the logic element?
  - Does the basic logic element contain a FF? What type?
- Interconnect
  - How fast is it? Does it offer ‘high speed’ paths that cross the chip? How many of these?
  - Can I have on-chip tri-state busses?
  - How routable is the design? If 95% of the logic elements are used, can I route the design?
  - More routing means more routability, but less room for logic elements

Issues in FPGA Technologies (cont)
- Macro elements
  - Are there SRAM blocks? Is the SRAM dual ported?
  - Is there fast adder support (i.e. fast carry chains?)
  - Is there fast logic support (i.e. cascade chains)
  - What other types of macro blocks are available (fast decoders? register files?)
- Clock support
  - How many global clocks can I have?
  - Are there any on-chip Phase Logic Loops (PLLs) or Delay Locked Loops (DLLs) for clock synchronization, clock multiplication?
Issues in FPGA Technologies (cont)

- What type of IO support do I have?
  - TTL, CMOS are a given
  - Support for mixed 5V, 3.3v IOs?
    - 3.3 v internal, but 5V tolerant inputs?
  - Support for new low voltage signaling standards?
    - GTL+, GTL (Gunning Transceiver Logic) - used on Pentium II
    - HSTL - High Speed Transceiver Logic
    - SSTL - Stub Series-Terminate Logic
    - USB - IO used for Universal Serial Bus (differential signaling)
    - AGP - IO used for Advanced Graphics Port
- Maximum number of IO? Package types?
  - Ball Grid Array (BGA) for high density IO

Altera FPGA Family Summaries

- Altera Flex10K/10KE
  - LEs (Logic elements) have 4-input LUTS (look-up tables)
  - 1 FF
  - Fast Carry Chain between LE’s, Cascade chain for logic operations
  - Large blocks of SRAM available as well
- Altera Max7000/Max7000A
  - EEPROM based, very fast (Tpd = 7.5 ns)
  - Basically a PLD architecture with programmable interconnect.
  - Max 7000A family is 3.3 v

Xilinx FPGA Family Summaries

- Virtex Family
  - SRAM Based
  - Largest device has 1M gates
  - Configurable Logic Blocks (CLBs) have two 4-input LUTS, 2 DFFs
  - Four onboard Delay Locked Loops (DLLs) for clock synchronization
  - Dedicated RAM blocks (LUTs can also function as RAM).
  - Fast Carry Logic
- XC4000 Family
  - Previous version of Virtex
  - No DLLs, No dedicated RAM blocks

Xilinx Virtex II Family

- Virtex II is Xilinx’s latest & greatest
- New technology:
  - embedded multipliers 18x18=36 bit, 2’s complement (signed multiplier)
  - Differential serial IO
  - Multiplier inputs are linked to embedded SRAM outputs for speed.
    - Extended to be used for digital filter applications where sample coefficient values are stored in the SRAM
  - A FIR filter (finite impulse response) equation has the form
    \[ y = x \cdot a_0 + x[1] \cdot a_1 + x[2] \cdot a_2 + \ldots + x[N-1] \cdot a_{N-1} \]
    The ‘x’ values are previous sample values (x[1] is one sample back), the ‘a’ values are coefficient.

Actel FPGA Family Summaries

- MXDS Family
  - Fine grain Logic Elements that contain Mux logic + DFF
  - Embedded Dual Port SRAM
  - One Time Programmable (OTP) - means that no configuration loading on powerup, no external serial ROM
  - AntiFuse technology for programming (AntiFuse means that you program the fuse to make the connection).
    - Fast (Tpd = 7.5 ns)
    - Low density compared to Altera, Xilinx - maximum number of gates is 36,000
Actel ProAsic basic logic module

Extremely primitive logic module (fine-grain architecture). Mux is basic building block – two muxes shown can implement a DFF via a master/slave latch arrangement.

Cypress CPLDs

- Ultra37000 Family
  - 32 to 512 Macrocells
  - Fast (Tpd 5 to 10ns depending on number of macrocells)
  - Very good routing resources for a CPLD