Stratix FPGA Homework

Compare Altera Stratix and FLEX families in several areas.

Basic mechanism for implementing random logic is the Logic Element which contains a 4-input Lookup Table + DFF. This has not changed much between families.

One difference is that Stratix added synchronous load and clear logic to every LE; this is a common functionality to have in register which was implemented as part of the LUT4 logic in the FLEX10K.

Also, old ‘cascade’ function in FLEX for wide AND/OR functions generalized in Stratix by allowing LUTs to chained together for wide functions (chain input is dedicated route between logic elements).

Fast Addition/Subtraction

Fact: The speed of carry generation determines speed of adder for binary addition.

FLEX10K had carry logic in each LE and dedicated carry chain routing between LEs to speed up carry propagation so that LUT4 and programmable routing did not have to be used for carry logic.

Stratix does several things to make addition and adder/subtractor faster and more efficient.

Adder/Subtractor Operation

A – B = A + B’ + 1

Carry-Select Adder

The Carry path is the slowest path in the ripple carry adder. We can speed it up with the following scheme (8-bit adder):

New to Stratix LE.

Used for building adder/subtractor, do not have to use LUT logic for this -- will speed up the operation and be more efficient in terms of resource usage.
Carry-Select Adder (larger N)


\[ \begin{array}{c|c|c|c}
\text{Rpl} & \text{A}\[3:0]\text{B}\[3:0] & \text{Cin} & \text{Sum}\[3:0] \\
\hline
0 & 0 & 0 & 0 \\
1 & 1 & 0 & 1 \\
\end{array} \]

Note that in this mode, LUT4 split into four 2-input LUTs, for computing sum bits with carry-in = 0, 1 and computing carry outs for carry-in = 0, 1.

Higher Level Arithmetic Support

- Flex10K had no support for higher level arithmetic support other than implementation as a netlist of LUT4s.
- Stratix has monolithic multipliers which can be configured as 9x9 or 18x18 multipliers. Four 18x18 multipliers can be used with a dedicated adder to form a 36x36 multiplier.

Multiplier sub-blocks are embedded in a DSP block. Output of multipliers to adder block that can be used for accumulation.

An interesting omission is that the DSP block cannot do saturating arithmetic.

Accumulator can be up to 52 bits (36 bit product from 18x18, plus 16 bits of accumulation).
SRAM Comparison

Flex10K: 2Kb single port SRAM blocks, configured as 256x8, 512x4, 1024x2, or 2048x1. Any dual port SRAM support is strictly multi-cycle dual port SRAM.

Stratix: three different blocks sizes available 512b, 4Kb, and one large block whose size is dependent upon the part. True Dual Port SRAM available.

In dual port modes, widths of the ports can be different.
Clocking Comparison
Flex 10K: each LE can select 1 of 2 global clocks. PLL provides clock multiplication by 2, and also syncs internal clock edges to external clock edges.

Stratix: Hierarchical clocking scheme, 16 global clock networks, driven by 4 enhanced PLLs. 16 regional clocks (4 per device quadrant), and 8 dedicated fast regional clock networks.

Clock Frequency Scaling: \( m/(n \times \text{post-scale counter}) \) where \( m, n, \) and post-scale counter all go from 1 to 512. \( M, N \) used for clock frequency, post-scale counter controls duty cycle.

Clock Skew
We have used the equation:
\[
\text{reg-to-reg delay} = C2q + \text{MaxCombDelay} + Tsu
\]
It is actually:
\[
\text{reg-to-reg delay} = C2q + \text{MaxCombDelay} + Tsu + Tskew
\]
Where \( Tskew \) is the clock skew. Clock skew is the difference in arrival times of clock edges at DFFs on the device.

\( Tskew \) is determined by die size, propagation delay across chip. Gate delays used to be large compared to \( Tskew \), so could ignore. As transistor lengths have scaled down, gates have gotten faster and can no longer ignore \( Tskew \).

Why Hierarchical Clocks?
Why have global, regional and fast regional clocks?
Because can specify different skews on the two clock networks – regional clocks will have smaller skew than global clocks, so any register-to-register paths clocked only by a regional clock can have tighter timing than a register to register path that crosses a regional boundary.

Can also save power

Regional clocks are associated with a particular chip quadrant.

Fast Regional Clocks
Suggested uses for fast regional clocks are high fanout signals like synchronous loads/clears, clock enables.
IO Technology

- Input/Output (IO) has become very complex
  - Used to only have to worry about TTL vs CMOS
  - TTL had current drive requirements, CMOS just voltage level requirements
  - Both used full swing signals (0 to Vdd, used to be 5 V)
- New issues in IO technology
  - Limit voltage swing to speed up signaling
  - Voltage swing about a reference voltage instead of between 0 and Vdd
  - Differential signaling to reject noise
  - Termination required to prevent signal reflections from corrupting signals

Classification of Advanced IO standards

- Single Ended- Full swing signals between 0 and VCCIO, tolerant of overdrive of input signals, various current drive capability
  - LVTTL, LVCMOS – tolerant of 5V overdrive, expects 3.3 V
  - 2.5V, 1.8V, 1.5V – simply lower voltage versions of LVTTL, LVCMOS
  - PCI 3.3V, PCI-X 3.3V – expects 3.3 V input signals, used to limit signal overshoot. But makes the pin intolerant of any drive that is over the clamping limit unless external series resistor used to limit current.

Stratix supported IO standards

<table>
<thead>
<tr>
<th>IO Standard</th>
<th>Type</th>
<th>Input Reference Voltage (Vref) (V)</th>
<th>Output Swing Voltage (Vout) (V)</th>
<th>Board Termination Voltage (Vint) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVCMOS</td>
<td>Single ended</td>
<td>3.3</td>
<td>3.3</td>
<td>N/A</td>
</tr>
<tr>
<td>3.3V</td>
<td>Single ended</td>
<td>3.3</td>
<td>3.3</td>
<td>N/A</td>
</tr>
<tr>
<td>1.5V</td>
<td>Single ended</td>
<td>1.5</td>
<td>1.5</td>
<td>N/A</td>
</tr>
<tr>
<td>1.8V</td>
<td>Single ended</td>
<td>1.8</td>
<td>1.8</td>
<td>N/A</td>
</tr>
<tr>
<td>2.5V</td>
<td>Single ended</td>
<td>2.5</td>
<td>2.5</td>
<td>N/A</td>
</tr>
<tr>
<td>3.3V</td>
<td>Single ended</td>
<td>3.3</td>
<td>3.3</td>
<td>N/A</td>
</tr>
<tr>
<td>LVDS/MLL</td>
<td>Differential</td>
<td>N/A</td>
<td>5.0</td>
<td>N/A</td>
</tr>
<tr>
<td>3.3V</td>
<td>Differential</td>
<td>3.3</td>
<td>3.3</td>
<td>N/A</td>
</tr>
<tr>
<td>2.5V</td>
<td>Differential</td>
<td>2.5</td>
<td>2.5</td>
<td>N/A</td>
</tr>
<tr>
<td>1.8V</td>
<td>Differential</td>
<td>1.8</td>
<td>1.8</td>
<td>N/A</td>
</tr>
<tr>
<td>1.5V</td>
<td>Differential</td>
<td>1.5</td>
<td>1.5</td>
<td>N/A</td>
</tr>
<tr>
<td>Level Shifter</td>
<td>LVDS to LVDS</td>
<td>3.3</td>
<td>3.3</td>
<td>N/A</td>
</tr>
<tr>
<td>3.3V</td>
<td>LVDS to LVDS</td>
<td>3.3</td>
<td>3.3</td>
<td>N/A</td>
</tr>
</tbody>
</table>

Notes for Table 32:
(a) The IOCL, IOOH, and IOH pins can be driven with signals higher than VCCIO.
(b) LVTTL/3.3V, LVTTL/1.8V, and LVTTL/1.5V drive devices with 3.3V tolerant input.
(c) LVTTL/1.5V, LVTTL/1.8V, and LVTTL/2.5V drive devices with 3.3V tolerant input.
(d) “0” means the device is not driven by a state machine, and the output is in the logic-low state.
(e) “1” means the device is driven by a state machine, and the output is in the logic-high state.

Clamping diode can be turned off/on for each IO, clamp to VCCIO. The VCCIO is the voltage of IO, and can be different from the supply voltage!!!!

Supply Voltage (VCCINT) always 1.5V.

Drive Strength control needed for current requirements of different IO standards
Classification of Advanced IO standards (cont)
- Voltage Referenced - Reduced voltage swing signals with differential receiver that compares input signal versus a reference voltage (Vref). Requires termination resistor tied to Vtt.

\[ \text{Vref} \pm \text{Vswing} \]

Vswing usually 10’s of millivolts to a few hundred millivolts. Vtt can be external to Receiver or internal. Vref can be supplied external or internal.

Why Voltage Referenced Signaling?
Smaller voltage swing means faster signaling.
Smaller voltage swing also means less current drive required.
Can be susceptible to noise.
Gunning Transceiver Logic (GTL) is one of the supported standards, used on the Pentium III/III/IV busses. Vtt = 1.5V, Vref = 1.0, voltage swing is +/- 200 mv about Vref.

Classification of Advanced IO standards (cont)
- Differential – two pairs of wires used to send a ‘1’ or ‘0’ - when D0+ > D0-, then a ‘1’ level. When D0+ < D0-, then a ‘0’ level. Typical differences in are in the few hundred millivolts.

Why differential signaling??
Differential signaling very good at rejecting common-mode noise. If noise is coupled into a cable, then usually it is coupled into all wires in the cable. This ‘common-mode’ noise (Vcm) can be rejected by input amplifier.

\[ V_o = (D^+) - (D^-) \]
\[ V_o = (V_{cm} + D^+) - (V_{cm} + D^-) \]

On Chip Termination
High speed signaling can cause reflections if line is not properly terminated (termination impedance matches source impedance).
Rule of thumb:
Reflections a problem when rise/fall time of signal is greater than 1/2 signal propagation delay along wire.
HyperTransport Differential Standard

HyperTransport is one of the supported differential standards. Each data line is actually a pair of lines. HyperTransport uses a source-synchronous protocol – a clock is transmitted along with the data. The clock is differential, same as the data. Speeds are 400 MT/s (million transfers), 600 MT/s, 800 MT/s, 1.0 GT/s, 1.2 GT/s, 1.6 GT/s. Bits/sec depends on number of data lines.

HyperTransport Clocking

Clock delayed by ½ bit time, so just latch data on crossing of clock signals. Valid data on CAD lines at clock crossings.

What is source-synchronous?

Traditional Synchronous (common-clock).

Backplane bus

Clock source comes from one global location, receiver/transmitter share the same clock.

Clock edge has different arrival times at data source/sinks due to different interconnect lengths (clock skew).

Setting worst case allowable clock skew limits interconnect length.

What is source-synchronous? (cont.)

Clock sent with data. Interconnect length does not matter because data, clock travels same distance and arrives at same time.

Double Data Rate Support

Double Data Rate interfaces transfer data on both clock edges.
Flex vs. Stratix: Key Differences

- Logic Element: Synchronous clr/preset built in, generalized cascade
- Addition/Subtraction: carry-select adder support, subtraction support in LE with XOR gate
- Other arithmetic: monolithic multipliers, DSP blocks with monolithic multipliers + adder for efficient multiply accumulate, multiply-sum
- SRAM: true dual port capability.
- Clocking: Hierarchical clock network with three levels of clocking (global, regional, fast regional)
- IO – support for new voltage-referenced and differential standards.

Altera Stratix vs. Xilinx Virtex II

- Logic elements are equivalent
- Virtex does not have carry-select adder support
- Virtex has monolithic multipliers (only 18x18 signed), but not DSP blocks (monolithic adder).
- Virtex does not have hierarchical clock network
- Both have true dual port RAM
- Both support the same IO standards.