Simulation and Modeling for Signal Integrity and EMC

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Outline

• Why Simulation?
  —Examples
• Simulation and signal integrity
• General-purpose analog simulators
• Transmission-line simulators
• Modeling for simulation
• Model standards
• Creating accurate models
• Simulation and signal integrity revisited
• Summary
Why Simulation?

- Example: Ringing and EMI (far field) on one trace
- Round-trip time, ringing, and EMC
- Solving SI problems can reduce EMC problems

Simulate to validate design (ideal world).
Why Simulation?

- Example: Ringing and EMI (far field) on one trace
- Edge rate, ringing and EMC
- Solving SI problems can reduce EMC problems

Simulate to find (and solve) problems (real world).
Why Simulation?

- Example: Crosstalk (near-field coupling) between traces
- Prevent forward and backward crosstalk
- Changing stackup can minimize crosstalk
- Moving traces to another routing layer can minimize problems related to crosstalk

*Simulate to compare tradeoffs during product design.*
Why Simulation?

Simulation = Virtual Prototyping

• Simulation allows one to prototype hardware using software (optimize terminations, correcting net list errors, …)

• *Plus*
  Analyze changes in stackup assignment/dimensions, run best/worst-case timing analysis, add/move vias, add/move/remove test points, add/move decoupling caps, …)
Why Simulation?

- Shorter and more predictable design cycles
- Fewer prototype turns
- Lower development cost means lower product cost
- Faster time to market
Simulation and Signal Integrity

Pre-Layout Analysis:

- SI and EMC design specifications
- Good constraints up front makes layout faster
- Better initial placement, less ripup/reroute
- Simulate to develop rules of thumb
- Validate existing rules of thumb
- Generate constraint values for routers
Simulation and Signal Integrity

Post-Layout Analysis:

• Problem solving on actual routed designs
• Identify “risk” to focus design efforts
• Optimize termination methodology
• Optimize I/O drivers
  (strength and slew rate options)
Simulation and Signal Integrity

**Modeling solid planes**
- Ideal plane approximation
- Cutouts, vias, and other complications
- Impacts simulation for some frequencies

**General analog simulator**
- Ground is a universal node for simulation analysis

**SI/EMC**
- “Layout ground” is a solid plane
- Layout ground is a REFERENCE VOLTAGE POINT
Simulation and Signal Integrity

Choosing the right type of simulator

- General purpose
- Transmission line
- Behavioral
- Combined simulation capability

Choosing correct models

- SPICE-style transistor parameters
- IBIS
- IBIS-X
- VHDL/AMS and Verilog/AMS
General-Purpose Analog Simulators

“SPICE” simulators
- Berkeley SPICE 2G6
- Berkeley updates
- Commercial SPICE (such as HSPICE)

Other general-purpose analog simulators
- Analogy/Avanti Sabre (MAST modeling language)
- Other non-SPICE algorithms
General-Purpose Analog Simulators

**Models**
- SPICE 2G6 netlists for structural relationships
  - Examples: op amp subcircuits, I/O subcircuits
  - SPICE 2G6 parameter lists for device modeling
  - Proprietary models and modeling languages
    (e.g. BSIM3V3 enhancements)
Transmission-Line Simulators

Many vendors supporting the IBIS standard
- Transmission lines usually supported in general-purpose (SPICE) simulators

Different from general-purpose simulators
- Optimized for transmission-line analysis
- Uncoupled lines or many coupled lines
- Lines of various lengths (time stepping)
- Often faster than SPICE (10x or more)
Transmission-Line Simulators

Models

- Topology “netlists” for structural relationships
- IBIS models for I/O buffers
- Proprietary models and modeling languages
Other Types of Simulators

*Digital timing/delay simulators*
- Delay through integrated circuits or modules
- Delay for interconnects
- Best/worst case timing analysis
- Can handle multiple paths between two pins

*Models*
- Netlist for structural relationships
- Logical relationships for pins
- Lists of valid paths and test vectors
Modeling for Simulation

**Time-domain models**
- Current = $f$ (node voltages)
- Current = $f$ (charge, voltage, state variables)
- Functions can include integrals and derivatives

**Frequency-domain models**
- LaPlace formulation
- Example: transmission line
  
  $\frac{V_{out}}{V_{in}} = \exp(-\alpha L) \exp(-st)$
- Polynomial vs. exponential equations
Modeling for Simulation

Model formats

- Subcircuits: easy to create, runs slow
- Equations: hard to create, can run fast (slow if iterative)
- Tables: easy to create, runs very fast

Tradeoffs in modeling

- What format(s) are supported by the simulator?
- Ease of creation vs. run time?
- Can the model be reused (parameterized)?
- Can models be created from measurements?
Model Standards

**SPICE 2G6**
- Structural netlist format
- Accepted by general-purpose analog simulators
- Other SPICE netlists may not be portable

**SPICE Models**
- Model equations usually coded into simulator
- Implementation often proprietary
- Subcircuits are structural (lists of components)
Model Standards

Component Models
- Component model = equations + parameters
- Model equations may be proprietary
- Model parameters often proprietary (e.g. foundry)

A SPICE model can (and will) produce different results on different simulators.
Model Standards

IBIS

- ANSI/EIA 656 – portable across different vendors
- I/O Buffer Information Specification (drivers and receivers)
- No circuit information ($I/V$ and $V/t$ tables for pins)
- Topology netlists are simulator-specific
  (not part of the standard)
- IBIS 3.2: EBD (Electrical Board Description)
Model Standards

IBIS-X

- Extending IBIS models: macro-language
- Simulator control (trigger conditions)
- Data patterns and relative switching times
- Many other enhancements
Model Standards

**VHDL and Verilog**
- Digital and mixed-signal structural description
- Digital functional behavior

**VHDL/AMS and Verilog/AMS**
- Mixed-signal structural description
- Digital functional behavior (logic functions)
- Analog functional behavior (equations)
- Triggers/values pass between digital and analog sections
Simulator Tradeoffs

*General Purpose Analog Simulators*
+ Handles a variety of analog components
- May not handle IBIS or other digital components
- Slow for transmission lines

*Transmission Line Simulators*
+ Very fast for transmission lines
- May not handle SPICE models

*Digital Delay/Timing Simulators*
+ Very fast, handles many nets
- May not handle analog models
Modeling Tradeoffs

**SPICE (and other analog models)**
- Models coded into simulator
- Not a standard; not portable across vendor platforms
- Equations are “compiled” within the simulator

**IBIS and IBIS-X**
- ANSI/EIA standard; portable
- Thousands available on the web

**VHDL/AMS & Verilog/AMS**
- ANSI/EIA standard; portable
- Few models available for I/O buffers
Creating Accurate Models

**The Silicon Foundry**
- Runs device and process simulations
- Generates SPICE transistor models

**I/O Designers**
- Circuit simulation using foundry models
- Extract IBIS model tables from SPICE simulations

**IBIS models can also be created from measurements**
- An IBIS model is a set of V/I and V/t tables
- Need enough samples for min/max values
Creating Accurate Models

Remember:
**Always validate models before you use them!**
Simulation and Signal Integrity/EMC Revisited

Pre-layout and post-layout

- Predicting effects of electrical changes
- Predicting effect of layout changes
- Simulating for SI and EMC
  — Single nets, groups of nets, coupled nets
Simulation and Signal Integrity/EMC Revisited

Making the right choices

- Simulator
- Models
- Methodology

**Validate methodology as well as models.**
Summary

There are two ways to solve problems:

- Reactive (ignore it and maybe it will go away)
- Proactive (before it gets more expensive to fix)

Was it cost-effective?

- Did it reduce prototype turns?
- Did it reduce product cost?
- Did it save on time-to-market?
Did you avoid doing that design over

instead of

- or in addition to -

moving on to the next project?