Verilog Transistor Modeling

- Verilog has both unidirectional and bidirectional transistor models for switch-level CMOS modeling.
  - Unidirectional:
    - `nmos`, `pmos` are unidirectional (three terminals).
    - `cmos` is a pass transistor – an `nmos`, `pmos` connected back to back (four terminals).
    - Strength reduction versions are `rnmos`, `rpmos`, `rcmos`.
  - Bidirectional, non-strength reducing:
    - `tranif0`, `tranif1` are bidirectional (three terminals).
    - Strength reducing versions are `rtranif0`, `rtranif1`.

Y = A xor B

\[ \begin{align*}
Y &= A \text{ xor } B \\
A &= B \\
B' &= Y
\end{align*} \]

\[ \text{module xorgate}(Y, A, B) ; \]

```
input A, B;
output Y;
supply0 gnd;
supply1 vdd;

// Inverter for internal Bnot
pmos p3 (BNOT, vdd, B);

nmos n3 (BNOT, gnd, B);

pmos p1 (Y, B, A);
nmos n1 (Y, BNOT, A);

pmos p2 (Y, A, B);
nmos n2 (Y, A, BNOT);

endmodule
```

Ramcell

To read, R = 1, W = 0, DIN = X.
To write '0': R = 1, W = 1, DIN = 1.
To write '1': R = 1, W = 1, DIN = 0.

DOUT latches last read or written value.

\[ \text{module ramcell}(dout, din, r, w) ; \]
```
input din, r, w;
output dout;
supply0 gnd;

not i3 (dinnot, din);
nmos tn1 (n5, gnd, dinnot);
nmos tn2 (n1, n5, w);
nmos tn3 (n6, gnd, din);

nmos tn4 (n4, n6, w);
nmos tn5 (n2, n1, r);
tranif1 tn6 (n4, n5, r);

not (pull0, pull1) i1(n3, n2);
not (pull0, pull1) i2(n2, n3);

not i4(dout, n4);
not (weak0, weak1) i5(n4, dout);

endmodule
```

Dynamic Gates

- Ntree

\[ \text{Precharge Transistor} \]
\[ \text{Logic Function (Pulldown network)} \]
\[ \text{Evaluation Transistor} \]

Note: Cannot specify drive strength on transistors!
Operation of a Dynamic Gate

- **Precharge phase**: Clock LOW, Precharge transistor on, output pull high. Evaluation transistor off.

  ![Precharge Diagram]

- **Evaluation phase**: Clock HIGH, Precharge transistor off, Evaluation transistor on. Output is pulled low if there is a path in Ntree to ground.

  ![Evaluation Diagram]

### Why must gate input only make a single low to high transition or remain high?

- **Equivalent to**: Dynamic gate equivalent to a static gate.

  ![Dynamic vs Static Diagram]

- **Input A makes a low to high transition, output charge already drained to ground when A went low to high.**

  ![Input Transition Diagram]

### Domino AND2 gate

- **Module**:

```verilog
module dom_and2(y, a, b, clk);
  output y;
  input a, b, clk;
  supply0 gnd;
  supply1 vdd;
  trireg(medium) yn;
  pmos tp1 (yn, vdd, clk);
  nmos tn1 (n1, gnd, clk);
  nmos tn2 (n2, n1, a);
  nmos tn3 (yn, n2, b);
  not i0 (y, yn);
  endmodule
```

- **Simulation**: Drive strength of yn internal node is "me1" node yn gets pulled to ST0, so output is ST1.

### Simulation of Domino AND2 gate
Simulation of Domino AND2 gate without trireg node

drive strength of yn internal node is now ‘HiZ’, which makes output a ‘StX’.

Simulation of illegal transition on A, B inputs

A, B go high, then drop low. Output goes to ‘1’ when both ‘A’, ‘B’ = 1, but then internal charge is drained so output remains at ‘1’ even when A, B return to ‘0’.

Subthreshold Leakage

• If the clock stays high for an extended period, the output charge will leak off due to subthreshold currents
• Dynamic circuits typically have a minimum clock frequency requirement because of this.
• Subthreshold leakage gets worse as you scale down in technology.
• A trireg net can have three delay values
  – (rise_delay, fall_delay, charge_decay_time)
  – charge_decay_time is time it takes for charge to decay to an ‘X’ value.

Domino Buffer with Charge Delay

module dom_buf(y, a, clk);
  output y;
  input a, clk;
  supply0 gnd;
  supply1 vdd;
  trireg(medium) #(0, 0, 40) yn;
  pmos tp1 (yn, vdd, clk);
  nmos tn1 (n1, gnd, clk);
  nmos tn2 (yn, n1, a);
  not i0 (y, yn);
endmodule

Simulation with Charge Delay

From 100 ns, Clk remains high.
After 40 ns, charge (Me1) decays to X value (MeX)
Output goes to StX